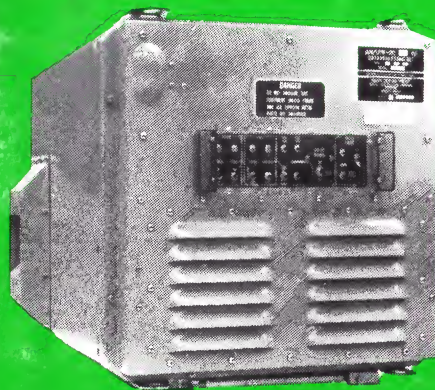




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AN/UYK-20 ISEA

# AN/UYK-20/20A

## Technical Summary



MAY 1991

# TABLE OF CONTENTS

Title	Page
AN/UUK-20 and AN/UUK-20A Computer Repertoire of Instructions	1
List of Nomenclature Items	11
List of Micro Memory Items	12
Current Line Replaceable Assemblies	13
Current AN/UUK-20 PC Card Placement Map	16
Current AN/UUK-20A PC Card Placement Map	17
Current Input/Output PC Card Assemblies	18
Power Supply Data	19
I/O Connector Panel	21
DPS I/O Connectors	24
Power Connector Data	27
Available NDRO Program Kit Configurations	28
Common Serial I/O Operating Mode Selection Instructions	38
AN/UUK-20 I/O Mode Selection Card	42
AN/UUK-20A I/O Mode Selection Card	43
AN/UUK-20 Retrofit Definition	46
AN/UUK-20 Publications, Equipment, and Program Tapes Required	47
AN/UUK-20A Publications, Equipment, and Program Tapes Required	49
Replaceable Assemblies—List	51
Diagnostic Operating Procedures (Micro and CP/Memory)	57
Diagnostic Operating Procedures (I/O and Options)	58
Micro Diagnostic with End-Around Jumpers Operating Procedure	60

AN/UYYK-20 & AN/UYYK-20A COMPUTER  
REPERTOIRE OF INSTRUCTIONS

OCTAL FORMAT o f a m	HEXIDECIMAL FORMAT OP a m	CODING FORMAT	INSTRUCTION	OPERATION	C DV CC
00 0 - -	00 - -	-	Diagnostic return	If diagnostic jump set R17 - $\mu P$	- NC -
00 3 a m	03 a m	BL a,y,m	Byte Load	(Y) byte -> R <sub>a</sub> ; 0 -> R <sub>a</sub> 15-8	0 0 X
01 0 a m	04 a m	LR a,m	Load (Register)	(R <sub>m</sub> ) -> R <sub>a</sub>	0 0 X
01 1 a m	05 a m	LX a,m	Load (Indirect)	(Y*) -> R <sub>a</sub>	0 0 X
01 2 a m	06 a m	LK a,y,m	Load (Constant)	Y -> R <sub>a</sub>	0 0 X
01 3 a m	07 a m	L a,y,m	Load	(Y) -> R <sub>a</sub>	0 0 X
02 0 a 00	08 a 0	PR a	Make positive	If (R <sub>a</sub> ) < 0, (R <sub>a</sub> )' -> R <sub>a</sub>	X X X
02 0 a 01	08 a 1	NR a	Make negative	If (R <sub>a</sub> ) > 0, (R <sub>a</sub> )' -> R <sub>a</sub>	X X X
02 0 a 02	08 a 2	RR a	Round	(R <sub>a</sub> ) + (R <sub>a</sub> +1) 15 -> R <sub>a</sub> ④	X X X
02 0 a 04	08 a 4	TCR a	Two's Complement	(R <sub>a</sub> )' -> R <sub>a</sub>	X X X
02 0 a 05	08 a 5	TCOR a	Two's Complement Double	(R <sub>a</sub> , R <sub>a</sub> +1) -> R <sub>a</sub> , R <sub>a</sub> +1 ④	X X X
02 0 a 06	08 a 6	DCR a	One's Complement	(R <sub>a</sub> ) bit-by-bit complement -> R <sub>a</sub>	0 0 X
02 0 a 10	08 a 8	IROR a	Increase R <sub>a</sub> by 1	(R <sub>a</sub> ) + 1 -> R <sub>a</sub>	X X X
02 0 a 11	08 a 9	OROR a	Decrease R <sub>a</sub> by 1	(R <sub>a</sub> ) - 1 -> R <sub>a</sub>	X X X
02 0 a 12	08 a A	IRTR a	Increase R <sub>a</sub> by 2	(R <sub>a</sub> ) + 2 -> R <sub>a</sub>	X X X
02 0 a 13	08 a B	ORTR a	Decrease R <sub>a</sub> by 2	(R <sub>a</sub> ) - 2 -> R <sub>a</sub>	X X X
02 1 a m	09 a m	LDI a,m	Load Double (Indirect)	(Y*, Y*+1) -> R <sub>a</sub> , R <sub>a</sub> +1 ③	0 0 X
02 3 a m	0B a m	LD a,y,m	Load Double	(Y, Y+1) -> R <sub>a</sub> , R <sub>a</sub> +1 ③	0 0 X
03 0 a 00	0C a 0	ER a	Executive Return	Generate interrupt; (P)*1 -> R <sub>a</sub> ④	0 0 X
03 0 a 01	0C a 1	SSOR a	Store SR1	SR1 -> R <sub>a</sub>	0 0 X
03 0 a 02	0C a 2	SSTR a	Store SR2	SR2 -> R <sub>a</sub>	0 0 X
03 0 a 03	0C a 3	SCR a	Store Clock	(RTC register) 15:0 -> R <sub>a</sub>	0 0 X
03 0 a 04	0C a 4	LPR a	Load P	(R <sub>a</sub> ) -> P	- NC -
03 0 a 05	0C a 5	LSOR a	Load SR1	(R <sub>a</sub> ) -> SR1	- NA -
03 0 a 06	0C a 6	LSTR a	Load SR2	(R <sub>a</sub> ) -> SR2	- NC -
03 0 a 07	0C a 7	LCR a	Load RTC lower	(R <sub>a</sub> ) -> RTC register 15:0;	- NC -
03 0 00 10	0C 0 8	ECR	Enable Clock	Enable RTC reg. (countup and interrupt)	- NC -
03 0 00 11	0C 0 9	OCR	Disable Clock	Disable RTC reg. (countup and interrupt)	- NC -
03 0 a 12	0C a A	LEM a	Load and Enable Mon. clock	(R <sub>a</sub> ) - Mon. clock reg.; enable countdown and interrupt	- NC -
03 0 00 13	0C 0 B	OM	Disable Monitor clock	Disable Mon. clock reg. (countdown and interrupt)	- NC -
03 0 a 14	0C a C	LCRD a	Load and enable Clock Double	(R <sub>a</sub> , R <sub>a</sub> +1) - RTC; enable countup only ④	- NC -
03 0 a 15	0C a D	SCRD a	Store Clock Double	(RTC Register) -> R <sub>a</sub> , R <sub>a</sub> +1 ④ ⑤	0 0 X
03 0 00 16	0C 0 E	ECIR	Enable Clock Interrupt	Enable RTC overflow interrupt	- NC -
03 0 00 17	0C 0 F	DCIR	Disable Clock Interrupt	Disable RTC overflow interrupt	- NC -
03 3 a m	0F a m	LM a,y,m	Load multiple	(Y... Y+m-1) -> R <sub>a</sub> , R <sub>m</sub>	- NC -
04 0 a 00	10 a 0	SQR a	Square Root	$\sqrt{(R_a, R_a+1)} -> R_{a+1}$ ; Rem. -> R <sub>a</sub> ③	0 X X
04 0 a 01	10 a 1	RYR a	Reverse Register	Reverse (R <sub>a</sub> )	0 0 X
04 0 a 02	10 a 2	COT a	Count Ones	Number of binary ones in R <sub>a</sub> -> R <sub>a</sub> +1	- NC -
04 0 a 03	10 a 3	SFR a	Scale Factor	Shift (R <sub>a</sub> , R <sub>a</sub> +1) left until (R <sub>a</sub> ) 15 ③	- NC -
04 3 a m	13 a m	BLX a,y,m	Byte Load and index by 1	(Y) byte -> R <sub>a</sub> ; (R <sub>m</sub> +1) -> R <sub>m</sub> ②	0 0 X
05 0 a m	14 a m	SR a,m	Set Bit	1 -> (R <sub>a</sub> ) <sub>m</sub>	- NC -
05 1 a m	15 a m	LXI a,m	Load and index by 1 (Indirect)	(Y*) -> R <sub>a</sub> ; (R <sub>m</sub> +1) -> R <sub>m</sub> ②	0 0 X
05 3 a m	17 a m	LX a,y,m	Load and index by 1	(Y) -> R <sub>a</sub> ; (R <sub>m</sub> +1) -> R <sub>m</sub> ②	0 0 X
06 0 a m	18 a m	ZBR a,m	Zero Bit	0 -> (R <sub>a</sub> ) <sub>m</sub>	0 0 X
06 1 a m	19 a m	LXI a,m	Load Double Index by 2 (Indirect)	(Y*, Y*+1) -> R <sub>a</sub> , R <sub>a</sub> +1; ② ③ ④	0 0 X
06 3 a m	1B a m	LDX a,y,m	Load Double, index by 2	(Y*, Y*+1) -> R <sub>a</sub> , R <sub>a</sub> +1; (R <sub>m</sub> +2) -> R <sub>m</sub> ② ③ ④	0 0 X
07 0 a m	1C a m	CBR a,m	Compare Bit	Test bit m of R <sub>a</sub> for zero	0 0 X
07 1 00 00	1D 0 m	LPI m	Load PSW (Indirect)	(Y*, Y*+1, Y*+2) -> P, SR1, SR2;	- NA -
07 3 00 00	1F 0 m	LP y,m	Load PSW	enable power fault interrupt	- NA -
10 0 a m	20 a m	LRSR a,m	Logical Right Shift (Register)	Shift (R <sub>a</sub> ) right (R <sub>m</sub> ) 5:0 places, zero fill	0 0 X
10 2 a m	22 a m	LRS a,y,m	Logical Right Shift	Shift (R <sub>a</sub> ) right Y 5:0 places, zero fill	0 0 X
10 3 a m	23 a m	BS a,y,m	Byte Store	(R <sub>a</sub> ) 7:0 -> Y byte	- NC -
11 0 a m	24 a m	ASRS a,m	Algebraic Right Shift (Register)	Shift (R <sub>a</sub> ) right (R <sub>m</sub> ) 5:0 places, sign fill	0 0 X
11 1 a m	25 a m	SI a,m	Store (Indirect)	(R <sub>a</sub> ) -> Y*	- NC -
11 2 a m	26 a m	ARS a,y,m	Algebraic Right Shift	Shift (R <sub>a</sub> ) right Y 5:0 places, sign fill	0 0 X
11 3 a m	27 a m	S a,y,m	Store	(R <sub>a</sub> ) -> Y	- NC -
12 0 a m	28 a m	LRDR a,m	Logical Right Double shift (Register)	Shift (R <sub>a</sub> , R <sub>a</sub> +1) right (R <sub>m</sub> ) 5:0 places, zero fill ④	0 0 X
12 1 a m	29 a m	SDI a,m	Store Double (Indirect)	(R <sub>a</sub> , R <sub>a</sub> +1) -> Y*, Y*+1 ③	- NC -
12 2 a m	2A a m	LDR a,y,m	Logical Right Double shift	Shift (R <sub>a</sub> , R <sub>a</sub> +1) right Y 5:0 places, zero fill	0 0 X
12 3 a m	2B a m	SD a,y,m	Store Double	(R <sub>a</sub> , R <sub>a</sub> +1) -> Y, Y+1 ③	- NC -

③ Optional Math Pac Instructions ④ Count = 31 for all zeros or all ones. ⑤ If a/m ⑥ a,m,y must be even

⑦ if a ≠ m ⑧ cc set on R<sub>a</sub>+1 only ⑨ If Class II interrupts enabled

OCTAL FORMAT O A M	HEXIDECIMAL FORMAT OP A M	CODING FORMAT	INSTRUCTION	OPERATION	C	OV	CC
13 0 a m	2C a m	ARD a,m	Algebraic Right Double shift	Shift (Ra, Ra+1) right (Rm)5g places, sign fill	0	0	X
13 2 a m	2E a m	ARD a,y,m	Algebraic Right Double shift	Shift (Ra, Ra+1) right Y5g places, sign fill	0	0	X
13 3 a m	2F a m	SM a,y,m	Store Multiple	(Ra) ← Y; (Rm) ← Y; Y ← 0	-	NC	-
14 0 a m	30 a m	ALS a,m	Algebraic Left shift (Register)	Shift (Ra) left (Rm)5g places, zero fill	0	X	X
14 2 a m	32 a m	ALS a,y,m	Algebraic Left shift	Shift (Ra) left Y5g places, zero fill	0	X	X
14 3 a m	33 a m	BSX a,y,m	Byte Store, index by 1	(Ra)7g ← Ybyte; (Rm)+1 ← Rm	-	NC	-
15 0 a m	34 a m	CLS a,m	Circular Left shift (Register)	Shift (Ra, Ra+1) circularly left (Rm)5g places	0	0	X
15 1 a m	35 a m	SXI a,m	Store Index by 1 (Indirect)	(Ra) ← Y; (Rm)+1 ← Rm	-	NC	-
15 2 a m	36 a m	CLS a,y,m	Circular Left shift	Shift (Ra) circularly left Y5g places	0	0	X
15 3 a m	37 a m	SM a,y,m	Store, index by 1	(Ra) ← Y; (Rm)+1 ← Rm	-	NC	-
16 0 a m	38 a m	ALDR a,m	Algebraic Left Double shift (Register)	Shift (Ra, Ra+1) left (Rm)5g places, zero fill	0	X	X
16 1 a m	39 a m	SDXI a,m	Store Double Index by 2 (Indirect)	(Rm)+1 ← Y; Y ← 1; (Rm)+2 ← Rm	-	NC	-
16 2 a m	3A a m	ALO a,y,m	Algebraic Left Double shift	Shift (Ra, Ra+1) left Y5g places, zero fill	0	X	X
16 3 a m	3B a m	SDX a,y,m	Store Double, index by 2	(Ra, Ra+1) ← Y; Y ← 1; (Rm)+2 ← Rm	-	NC	-
17 0 a m	3C a m	CLDR a,m	Circular Left Double shift (Register)	Shift (Ra, Ra+1) circularly left (Rm)5g places	0	0	X
17 1 00 m	3D 0 m	SZI m	Store Zeros (Indirect)	Shift (Ra, Ra+1) circularly left Y5g places	-	NC	-
17 2 a m	3E a m	CLO a,y,m	Circular Left Double shift	Shift (Ra, Ra+1) circularly left Y5g places, zero fill	0	0	X
17 3 00 m	3F 0 m	SZY m	Store Zeros	Y ← 0	-	NC	-
20 0 a m	40 a m	SUB a,m	Subtract (Register)	(Ra) ← (Ra) - (Rb)	X	X	X
20 1 a m	41 a m	SUI a,m	Subtract (Indirect)	(Ra) ← (Y) - (Rb)	X	X	X
20 2 a m	42 a m	SUX a,y,m	Subtract (Constant)	(Ra) ← Y - (Rb)	X	X	X
20 3 a m	43 a m	SUI a,y,m	Subtract	(Ra) ← (Y) - (Rb)	X	X	X
20 4 a m	44 a m	SUD a,m	Subtract Double (Register)	(Ra, Ra+1) ← (Rm, Rm+1) - (Rb, Rb+1)	X	X	X
21 1 a m	45 a m	SUDI a,m	Subtract Double (Indirect)	(Ra, Ra+1) ← (Y, Y+1) - (Rb, Rb+1)	X	X	X
21 3 a m	47 a m	SUD a,y,m	Subtract Double	(Ra, Ra+1) ← (Y, Y+1) - (Rb, Rb+1)	X	X	X
22 0 a m	48 a m	AR a,m	Add (Register)	(Ra) ← (Ra) + (Rb)	X	X	X
22 1 a m	49 a m	AI a,m	Add (Indirect)	(Ra) ← (Y) + (Rb)	X	X	X
22 2 a m	4A a m	AK a,y,m	Add (Constant)	(Ra) ← Y + (Rb)	X	X	X
22 3 a m	4B a m	AR a,y,m	Add	(Ra) ← (Y) + (Rb)	X	X	X
23 0 a m	4C a m	ADR a,m	Add Double (Register)	(Ra, Ra+1) ← (Rm, Rm+1) + (Rb, Rb+1)	X	X	X
23 1 a m	4D a m	ADI a,m	Add Double (Indirect)	(Ra, Ra+1) ← (Y, Y+1) + (Rb, Rb+1)	X	X	X
23 3 a m	4F a m	AD a,y,m	Add Double	(Ra, Ra+1) ← (Y, Y+1) + (Rb, Rb+1)	X	X	X
24 0 a m	50 a m	CR a,m	Compare (Register)	(Ra) ← (Rm)	X	X	X
24 1 a m	51 a m	CI a,m	Compare (Indirect)	(Ra) ← (Y)	X	X	X
24 2 a m	52 a m	CK a,y,m	Compare (Constant)	(Ra) ← Y	X	X	X
24 3 a m	53 a m	CAR a,m	Compare	(Ra) ← (Y)	X	X	X
25 0 a m	54 a m	CDR a,m	Compare Double (Register)	(Ra, Ra+1) ← (Rm, Rm+1)	X	X	X
25 1 a m	55 a m	CDI a,m	Compare Double (Indirect)	(Ra, Ra+1) ← (Y, Y+1)	X	X	X
25 3 a m	57 a m	CD a,y,m	Compare Double	(Ra, Ra+1) ← (Y, Y+1)	X	X	X
26 0 a m	58 a m	MR a,m	Multiply (Register)	(Ra+1) ← (Ra) × (Rb, Rb+1)	X	X	X
26 1 a m	59 a m	MI a,m	Multiply (Indirect)	(Ra+1) ← Y × (Rb, Rb+1)	X	X	X
26 2 a m	5A a m	MK a,y,m	Multiply (Constant)	(Ra+1) ← (Y) × (Rb, Rb+1)	X	X	X
26 3 a m	5B a m	MA a,y,m	Multiply	(Ra+1) ← (Y) × (Rb, Rb+1)	X	X	X
27 0 a m	5C a m	DR a,m	Divide (Register)	(Ra, Ra+1) ← (Rm) - (Rb+1)	X	X	X
27 1 a m	5D a m	DI a,m	Divide (Indirect)	remainder ← Rb (Ra, Ra+1) ← (Y) - (Rb+1)	X	X	X
27 2 a m	5E a m	DK a,y,m	Divide (Constant)	(Ra, Ra+1) ← Y - (Rb+1) remainder ← Rb	X	X	X
27 3 a m	5F a m	D a,y,m	Divide	(Ra, Ra+1) ← (Y) - (Rb+1) remainder ← Rb	X	X	X
30 0 a m	60 a m	ANDR a,m	AND (Register)	(Ra) ← (Rm) & (Rb)	0	0	X
30 1 a m	61 a m	ANDI a,m	AND (Indirect)	(Ra) ← (Y) & (Rb)	0	0	X
30 2 a m	62 a m	ANDK a,y,m	AND (Constant)	(Ra) ← Y & (Rb)	0	0	X
30 3 a m	63 a m	AND a,y,m	AND	(Ra) ← (Y) & (Rb)	0	0	X
31 0 a m	64 a m	ORR a,m	OR (Register)	(Ra) ← (Rm)   (Rb)	0	0	X
31 1 a m	65 a m	OR I a,m	OR (Indirect)	(Ra) ← (Y)   (Rb)	0	0	X
31 2 a m	66 a m	ORK a,y,m	OR (Constant)	(Ra) ← Y   (Rb)	0	0	X
31 3 a m	67 a m	DR a,y,m	OR	(Ra) ← (Y)   (Rb)	0	0	X
32 0 a m	68 a m	XDRR a,m	Exclusive OR (Register)	(Ra) ← (Rm) ^ (Rb)	0	0	X
32 1 a m	69 a m	XDR I a,m	Exclusive OR (Indirect)	(Ra) ← (Y) ^ (Rb)	0	0	X
32 2 a m	6A a m	XDRK a,y,m	Exclusive OR (Constant)	(Ra) ← Y ^ (Rb)	0	0	X
32 3 a m	6B a m	XDR a,y,m	Exclusive OR	(Ra) ← (Y) ^ (Rb)	0	0	X
33 0 a m	6C a m	MSR a,m	Masked Substitute (Register)	II (Ra)17g ← 1; (Rm)17g ← Rb	0	0	X
33 1 a m	6D a m	MSI a,m	Masked Substitute (Indirect)	II (Ra)17g ← 1; (Y)17g ← Rb	0	0	X
33 2 a m	6E a m	MSK a,y,m	Masked Substitute (Constant)	II (Ra)17g ← 1; Y17g ← Rb	0	0	X
33 3 a m	6F a m	MS a,y,m	Masked Substitute	II (Ra)17g ← 1; (Y)17g ← Rb	0	0	X
34 0 a m	70 a m	CMR a,m	Compare Masked (Register)	II (Ra) & (Ra+1)   (Rm) & (Rm+1)	0	0	X

OCTAL FORMAT O A M	HEXIDECIMAL FORMAT OP A M	CODING FORMAT	INSTRUCTION	OPERATION	C	OV	CC
34 1 a m	71 a m	CMJ a,m	Compare Masked (Indirect)	II (Ra) & (Ra+1)   (Y) & (Y+1)	0	0	X
34 2 a m	72 a m	CMK a,y,m	Compare Masked (Constant)	II (Ra) & (Ra+1)   Y & (Y+1)	0	0	X
34 3 a m	73 a m	CM a,y,m	Compare Masked	II (Ra) & (Ra+1)   (Y) & (Y+1)	0	0	X
35 0 00 a	74 0 0	IOCR	Input/Output Command	Execute (I/O): 0 → 014015, 14	-	NC	-
35 1 00 a	75 0 0	BF m	Branch Fetch (Indirect)	(Y) ← CC; 1 → Y; 15, 14	0	0	X
35 2 00 a	76 0 0	RES a,y,m	Remainder Execute	Execute (Y)7g   Y7g ← 2	-	NA	-
35 3 00 a	77 0 0	BF a,y,m	Branch Fetch	(Y) ← CC; 1 → Y; 15, 14	0	0	X
437 0 a m	7C 0 a	See page 6	Top & Hyperbolic		-	NC	-
437 0 a 010	7C 0 8	FC a,y	Floating Point Compare	(Ra, Ra+1) ← (Y, Y+1)	0	0	X
437 0 a 011	7C 0 9	FXC a	Fixed to Floating Point Conversion	Fix normalized Floating Point number in Ra, Ra+1, from the binary exponent in Ra, and integer mantissa in Ra+1. (2's complement)	X	X	X
437 0 a 012	7C 0 A	FLC a	Floating Point to Fixed Conversion	Unpack Floating Point number in Ra, Ra+1 into binary exponent in Ra and integer mantissa into Ra+1	0	0	X
437 0 a 013	7C 0 B	NF a	Floating Point Normalize	Normalize the Floating Point number in Ra, Ra+1	X	X	X
437 0 a 016	7C 0 E	DAL a,y	Algebraic Left Double Shift	Shift (Ra, Ra+1, Ra+2, Ra+3) Left Y5g places, zero fill	0	0	X
437 0 a 017	7C 0 F	DAR a,y	Algebraic Right Double Shift	Shift (Ra, Ra+1, Ra+2, Ra+3) Right Y5g places, sign fill	0	0	X
40 0 00 m	80 0 0	JER m	Jump Equal	II CC indicates = or 0; (Rm) → P	-	NC	-
40 0 01 m	80 1 0	JNER m	Jump Not Equal	II CC indicates ≠ or not 0; (Rm) → P	-	NC	-
40 0 02 m	80 2 0	JGER m	Jump Greater or Equal	II CC indicates ≥ or +; (Rm) → P	-	NC	-
40 0 03 m	80 3 0	JLSR m	Jump Less	II CC indicates < or -; (Rm) → P	-	NC	-
40 0 04 m	80 4 0	JDR m	Jump Overflow	II overflow set: (Rm) → P	-	NC	-
40 0 05 m	80 5 0	JCR m	Jump Carry	II carry set: (Rm) → P	-	NC	-
40 0 06 m	80 6 0	JPT m	Jump Power out of Tolerance	II power out of tolerance: (Rm) → P	-	NC	-
40 0 07 m	80 7 0	JBR m	Jump Bootstrap 2 selected	II bootstrap 2 selected: (Rm) → P	-	NC	-
40 0 10 m	80 8 0	JR m	Jump	(Rm) → P	-	NC	-
40 0 11 m	80 9 0	JSR m	Jump after Stop	Stop; (Rm) → P	-	NC	-
40 0 12 m	80 A 0	JKSR 1,m	Jump, If Key set-Stop, then jump (Register)	If key 1 set, stop; (Rm) → P	-	NC	-
40 0 13 m	80 B 0	JKSR 2,m	Jump, If Key set-Stop, then jump (Register)	If key 2 set, stop; (Rm) → P	-	NC	-
40 1 d	81 d	LJ x0	Local Jump	(P) + 0 → P	-	NC	-
40 2 00 m	82 0 0	JE y,m	Jump Equal	II CC indicates = or 0; Y → P	-	NC	-
40 2 01 m	82 1 0	JNE y,m	Jump Not Equal	II CC indicates ≠ or not 0; Y → P	-	NC	-
40 2 02 m	82 2 0	JGE y,m	Jump Greater than or Equal	II CC indicates ≥ or +; Y → P	-	NC	-
40 2 03 m	82 3 0	JLS y,m	Jump Less	II CC indicates < or -; Y → P	-	NC	-
40 2 04 m	82 4 0	JO y,m	Jump on Overflow	II overflow set: Y → P	-	NC	-
40 2 05 m	82 5 0	JCY y,m	Jump on Carry	II carry set: Y → P	-	NC	-
40 2 06 m	82 6 0	JPT y,m	Jump If Power out of Tolerance	II power out of tolerance: Y → P	-	NC	-
40 2 07 m	82 7 0	JB y,m	Jump If Bootstrap 2 selected	II bootstrap 2 selected: Y → P	-	NC	-
40 2 10 m	82 8 0	JY y,m	Jump	Y → P	-	NC	-
40 2 11 m	82 9 0	JS y,m	Jump after Stop	Stop; Y → P	-	NC	-
40 2 12 m	82 A 0	JKS 1,y,m	Jump, If Key set-Stop, then jump	If key 1 set, stop; Y → P	-	NC	-
40 2 13 m	82 B 0	JKS 2,y,m	Jump, If Key set-Stop, then jump	If key 2 set, stop; Y → P	-	NC	-
40 3 00 m	83 0 0	JE y,y,m	Jump Equal	II CC indicates = or 0; (Y) → P	-	NC	-
40 3 01 m	83 1 0	JNE y,y,m	Jump Not Equal	II CC indicates ≠ or not 0; (Y) → P	-	NC	-
40 3 02 m	83 2 0	JGE y,y,m	Jump Greater or Equal	II CC indicates ≥ or +; (Y) → P	-	NC	-
40 3 03 m	83 3 0	JLS y,y,m	Jump Less	II CC indicates < or -; (Y) → P	-	NC	-
40 3 04 m	83 4 0	JO y,y,m	Jump on Overflow	II overflow set: (Y) → P	-	NC	-
40 3 05 m	83 5 0	JCY y,y,m	Jump on Carry	II carry set: (Y) → P	-	NC	-
40 3 06 m	83 6 0	JPT y,y,m	Jump If Power out of Tolerance	II power out of tolerance: (Y) → P	-	NC	-
40 3 07 m	83 7 0	JB y,y,m	Jump If Bootstrap 2 selected	II bootstrap 2 selected: (Y) → P	-	NC	-
40 3 10 m	83 8 0	JY y,y,m	Jump	(Y) → P	-	NC	-
40 3 11 m	83 9 0	JS y,y,m	Jump after Stop	Stop; (Y) → P	-	NC	-
40 3 12 m	83 A 0	JKS 1,y,y,m	Jump, If Key set-Stop, then jump	If key 1 set, stop; (Y) → P	-	NC	-
40 3 13 m	83 B 0	JKS 2,y,y,m	Jump, If Key set-Stop, then jump	If key 2 set, stop; (Y) → P	-	NC	-
41 0 a 0 m	84 a 0	XJB a,m	Index Jump Register	II (Ra) ≠ 0; (Ra) - 1 → Ra, (Rm) → P	-	NC	-
41 1 d	85 d	LJ x0	Local Jump (Indirect)	(P) + 0 → P	-	NC	-
41 2 a m	86 a m	XJ a,y,m	Index Jump	II (Ra) ≠ 0; (Ra) - 1 → Ra, Y → P	-	NC	-
41 3 a m	87 a m	XJ a,y,m	Index Jump	II (Ra) ≠ 0; (Ra) - 1 → Ra, (Y) → P	-	NC	-

# Optional Math Pac Instruction  
 a,m,y must be even      ? cannot be executed via execute remote      @ operands must be normalized

DECIMAL FORMAT o f a m	HEXIDECIMAL FORMAT OP a m	CODING FORMAT	INSTRUCTION	OPERATION	C OV CC
42 0 a m	88 a m	JLRR a,m	Jump, Link Register (Register)	$(P) + 1 \rightarrow R_0; (R_0) \rightarrow P$	- NC -
42 2 a m	8A a m	JLR a,y,m	Jump, Link Register	$(P) + 2 \rightarrow R_0; Y \rightarrow P$	- NC -
42 3 a m	8B a m	JLR a*,y,m	Jump, Link Register	$(P) + 2 \rightarrow R_0; (Y) \rightarrow P$	- NC -
43 1 d	8D d	LIJL d	Local Jump, Link Memory	$(P) + 1 \rightarrow (P); (P) + D + 1 \rightarrow P$	- NC -
43 2 00 m	8E 0 m	LIJM y,m	Jump, Link Memory	$(P) + 2 \rightarrow Y; Y + 1 \rightarrow P$	- NC -
43 3 00 m	8F 0 m	LIJM y,m	Jump, Link Memory	$(P) + 2 \rightarrow Y; (Y) + 1 \rightarrow P$	- NC -
44 0 a m	90 a m	JER a,m	Jump Zero (Register)	$I(R_0) = 0; (R_0) \rightarrow P$	- NC -
44 1 d	91 d	LJE d	Local Jump Equal	$I(R_0) \text{ indicates } = \text{ or } 0; (P) + D \rightarrow P$	- NC -
44 2 a m	92 a m	JZ a,y,m	Jump Zero	$I(R_0) = 0; Y \rightarrow P$	- NC -
44 3 a m	93 a m	JZ a*,y,m	Jump Zero	$I(R_0) = 0; (Y) \rightarrow P$	- NC -
45 0 a m	94 a m	JNZR a,m	Jump Not Zero (Register)	$I(R_0) \neq 0; (R_0) \rightarrow P$	- NC -
45 1 d	95 d	LINE d	Local Jump Not Equal	$I(R_0) \text{ indicates } \neq \text{ or not } 0; (P) + D \rightarrow P$	- NC -
45 2 a m	96 a m	JNZ a,y,m	Jump Not Zero	$I(R_0) \neq 0; Y \rightarrow P$	- NC -
45 3 a m	97 a m	JNZ a*,y,m	Jump Not Zero	$I(R_0) \neq 0; (Y) \rightarrow P$	- NC -
46 0 a m	98 a m	JPR a,m	Jump Positive (Register)	$I(R_0) \geq 0; (R_0) \rightarrow P$	- NC -
46 1 d	99 d	LIGE d	Local Jump Greater or Equal	$I(R_0) \text{ indicates } \geq \text{ or } +; (P) + D \rightarrow P$	- NC -
46 2 a m	9A a m	JP a,y,m	Jump Positive	$I(R_0) \geq 0; Y \rightarrow P$	- NC -
46 3 a m	9B a m	JP a*,y,m	Jump Positive	$I(R_0) \geq 0; (Y) \rightarrow P$	- NC -
47 0 a m	9C a m	JNR a,m	Jump Negative (Register)	$I(R_0) < 0; (R_0) \rightarrow P$	- NC -
47 1 d	9D d	LJLS d	Local Jump Less	$I(R_0) \text{ indicates } < \text{ or } -; (P) + D \rightarrow P$	- NC -
47 2 a m	9E a m	JN a,y,m	Jump Negative	$I(R_0) < 0; Y \rightarrow P$	- NC -
47 3 a m	9F a m	JN a*,y,m	Jump Negative	$I(R_0) < 0; (Y) \rightarrow P$	- NC -
# 50 0 a m	A0 a m	FSUH a,m	Floating point Subtract (Register)	$(R_0, R_{R+1}) \rightarrow (R_0, R_{R+1}) - R_0$	X X X
# 50 1 a m	A1 a m	FSUJ a,m	Floating point Subtract (Indirect)	$(R_0, R_{R+1}) \rightarrow (Y*, Y*+1) - R_0, R_{R+1}$	X X X
# 50 3 a m	A3 a m	FSU a,y,m	Floating point Subtract	$(R_0, R_{R+1}) \rightarrow (Y, Y+1) - R_0, R_{R+1}$	X X X
# 51 0 a m	A4 a m	FAR a,m	Floating point Add (Register)	$(R_0, R_{R+1}) \rightarrow (R_0, R_{R+1}) + R_0$	X X X
# 51 1 a m	A5 a m	FAI a,m	Floating point Add (Indirect)	$(R_0, R_{R+1}) \rightarrow (Y*, Y*+1) + R_0$	X X X
# 51 3 a m	A7 a m	FA a,y,m	Floating point Add	$(R_0, R_{R+1}) \rightarrow (Y, Y+1) + R_0, R_{R+1}$	X X X
# 52 0 a m	A8 a m	FMR a,m	Floating point Multiply (Register)	$(R_0, R_{R+1}) \rightarrow (R_0, R_{R+1}) \times R_0$	X X X
# 52 1 a m	A9 a m	FMI a,m	Floating point Multiply (Indirect)	$(R_0, R_{R+1}) \rightarrow (Y*, Y*+1) \times R_0$	X X X
# 52 3 a m	AB a m	FM a,y,m	Floating point Multiply	$(R_0, R_{R+1}) \rightarrow (Y, Y+1) \times R_0, R_{R+1}$	X X X
# 53 0 a m	AC a m	FOR a,m	Floating point Divide (Register)	$(R_0, R_{R+1}) \rightarrow (R_0, R_{R+1}) / R_0$	X X X
# 53 1 a m	AD a m	FOI a,m	Floating point Divide (Indirect)	$(R_0, R_{R+1}) \rightarrow (Y*, Y*+1) / R_0$	X X X
# 53 3 a m	AF a m	FO a,y,m	Floating point Divide	$(R_0, R_{R+1}) \rightarrow (Y, Y+1) / R_0, R_{R+1}$	X X X
*54 0 a m	B0 a m	LARR a,m	Load Address Register (Register)	$(R_0) \rightarrow AR_0$ SEE LEGEND	- NC -
*54 1 a m	B1 a m	LARI a,m	Load Address Register (Indirect)	$(Y*) \rightarrow AR_0$	- NC -
*54 3 a m	B3 a m	LARM a,y,m	Load Address Register Multiple	$(Y, \dots, Y + u) \rightarrow AR_0, \dots, AR_0 + u$	- NC -
*55 0 a m	B4 a m	SARR a,m	Store Address Register (Register)	$(AR_0) \rightarrow R_0$	- NC -
*55 1 a m	B5 a m	SARI a,m	Store Address Register (Indirect)	$(AR_0) \rightarrow Y*$	- NC -
*55 3 a m	B7 a m	SARM a,y,m	Store Address Register Multiple	$(AR_0, \dots, AR_0 + u) \rightarrow Y, \dots, Y + u$	- NC -
# 56 0 a m	B8 a m	MDR a,m	Multiply Double (Register)	$(R_{R+1}, R_{R+2}) \rightarrow (R_{R+1}, R_{R+2}) \times R_0$	0 0 X
# 56 1 a m	B9 a m	MDI a,m	Multiply Double (Indirect)	$(R_{R+1}, R_{R+2}) \rightarrow (Y*, Y*+1) \times R_0$	0 0 X
# 56 3 a m	BB a m	MO a,y,m	Multiply Double	$(R_{R+1}, R_{R+2}) \rightarrow (Y, Y+1) \times R_0, R_{R+1}$	0 0 X
# 57 0 a m	BC a m	DDR a,m	Divide Double (Register)	$(R_{R+1}, R_{R+2}) \rightarrow (R_{R+1}, R_{R+2}) / R_0$	0 0 X
# 57 1 a m	BD a m	DDI a,m	Divide Double (Indirect)	$(R_{R+1}, R_{R+2}) \rightarrow (Y*, Y*+1) / R_0$	0 0 X
# 57 3 a m	BF a m	DO a,y,m	Divide Double	$(R_{R+1}, R_{R+2}) \rightarrow (Y, Y+1) / R_0, R_{R+1}$	0 0 X
60 0 a m	C0 a m	LLRS a,m	Literal Logical Right Shift	Shift $(R_0)$ right $n$ places, zero fill	0 0 X
60 1 a m	C1 a m	LARS a,m	Literal Algebraic Right Shift	Shift $(R_0)$ right $n$ places, sign fill	0 0 X
60 2 a m	C2 a m	LLRD a,m	Literal Logical Right Shift	Shift $(R_0, R_{R+1})$ right $n$ places, zero fill	0 0 X

# Optional Math Pn Instructions ① a,y,m must be even

\*See Expanded Memory Legend

DECIMAL FORMAT o f a m	HEXIDECIMAL FORMAT DP a m	CODING FORMAT	INSTRUCTION	OPERATION	C OV CC
60 3 a m	C3 a m	LARD a,m	Literal Algebraic Right Shift	Shift $(R_0, R_{R+1})$ right $n$ places, sign fill ①	0 0 X
61 0 a m	C4 a m	LALS a,m	Literal Algebraic Left Shift	Shift $(R_0)$ left $n$ places, zero fill	0 0 X
61 1 a m	C5 a m	LCLS a,m	Literal Circular Left Shift	Shift $(R_0)$ left circular $n$ places, zero fill	0 0 X
61 2 a m	C6 a m	LALD a,m	Literal Algebraic Left Shift	Shift $(R_0, R_{R+1})$ left $n$ places, zero fill ①	0 0 X
61 3 a m	C7 a m	LCLD a,m	Literal Circular Left Shift	Shift $(R_0, R_{R+1})$ left circular $n$ places, ①	0 0 X
62 0 a m	C8 a m	LSU a,m	Literal Subtract	$(R_0) \rightarrow R_0 - R_0$	X X X
62 1 a m	C9 a m	LSUD a,m	Literal Subtract Double	$(R_0, R_{R+1}) \rightarrow R_0, R_{R+1} - R_0$	X X X
62 2 a m	CA a m	LA a,m	Literal Add	$(R_0) \rightarrow R_0 + R_0$	X X X
62 3 a m	CB a m	LAD a,m	Literal Add Double	$(R_0, R_{R+1}) \rightarrow R_0, R_{R+1} + R_0$	X X X
63 0 a m	CC a m	LL a,m	Literal Logical Right Shift	$m \rightarrow R_0$	0 0 X
63 1 a m	CD a m	LC a,m	Literal Circular Right Shift	$(R_0) \rightarrow R_0$	X X X
63 2 a m	CE a m	LMUL a,m	Literal Multiply	$(R_{R+1}) \rightarrow R_0, R_{R+1} \times R_0$	0 0 X
63 3 a m	CF a m	LDIV a,m	Literal Divide	$(R_{R+1}) / m \rightarrow R_{R+1}$	0 0 X
64 3 a m	D3 a m	BSU a,m	Byte Subtract	$(R_0) \rightarrow (Y) \text{ byte} - R_0$	X X X
65 3 a m	D7 a m	BA a,y,m	Byte Add	$(R_0) \rightarrow (Y) \text{ byte} + R_0$	X X X
66 3 a m	D8 a m	BC a,y,m	Byte Compare	$(R_0) \rightarrow (Y) \text{ byte}$	X X X
67 0 a m	DC a m	UMI a,m	User Macro - CP	Reserved for User Macro	-NA-
67 1 a m	DD a m	UMI a,m	User Macro - CP	Reserved for User Macro	-NA-
67 2 a m	DE a m	UMK a,y,m	User Macro - CP	Reserved for User Macro	-NA-
67 3 a m	DF a m	BCX a,y,m	Byte Compare and Index By 1	$(R_0) \rightarrow (Y) \text{ byte}; (R_0) + 1 \rightarrow R_0$	X X X
COMMAND/CHAIN INSTRUCTION					
70 0 00 00	E0 0 0	ACR 0	Channel Control	Master clear all channels	
70 0 00 04	E0 0 4	ACR 4	Channel Control	Enable external interrupts, all channels	
70 0 00 05	E0 0 5	ACR 5	Channel Control	Disable external interrupts, all channels	
70 0 00 06	E0 0 6	ACR 6	Channel Control	Enable Class III, Priority 2, 3, 4 interrupts	
70 0 00 07	E0 0 7	ACR 7	Channel Control	Disable Class III, Priority 2, 3, 4 interrupts	
70 0 a 10	E0 a 8	CCR,10	Channel Control	Master clear chan. a	
70 0 a 14	E0 a C	CCR a,14	Channel Control	Enable chan. a external interrupts	
70 0 a 15	E0 a D	CCR a,15	Channel Control	Disable chan. a external interrupts	
70 0 a 16	E0 a E	CCR a,16	Channel Control	Enable chan. a Class III, Priority 2, 3, 4 interrupts	
70 0 a 17	E0 a F	CCR a,17	Channel Control	Disable chan. a Class III, Priority 2, 3, 4 interrupts	
72 0 a m			User Macro - I/O	Reserved for User Macro	
72 1 a m			User Macro - I/O	Reserved for User Macro	
COMMAND INSTRUCTION					
71 2 a 02	E6 a 2	ICK a,y	Initiate Input Chain	Y - Channel a Chain Pointer; initiate input chain	
71 2 a 06	E6 a 6	OCK a,y	Initiate Output Chain	Y - Channel a Chain Pointer; initiate output chain	
71 2 a m	E7 a m	WM a,y,m	Write Control Memory	(Y) - Channel a CM <sub>0</sub> } use I/O	
72 3 a m	E8 a m	RIM a,y,m	Read Control Memory	Chan. a (CM <sub>0</sub> ) - Y } Page 8	
76 0 a m	F8 a m	SICR a,m	Serial Interface Control	Set or clear chan. a I/O discrete function	
76 3 a 00	F8 a 0	SST a,y	Serial Status	Channel a Serial Status bits - Y per Page 10	
CHAIN INSTRUCTION					
70 3 a 00	E3 0 0	IO 0,y	Input Data	(Y, Y+1) -> BWOC, BAP; initiate transfer	
70 3 a 01	E3 1 0	IO 1,y	Output Data	(Y, Y+1) -> BWOC, BAP; initiate transfer	
70 3 a 02	E3 2 0	IO 2,y	External Function	(Y, Y+1) -> BWOC, BAP; initiate transfer	
70 3 a 03	E3 3 0	IO 3,y	Force External Function	(Y, Y+1) -> BWOC, BAP; initiate transfer	
71 2 00 m	E6 0 m	LCMK m,y	Local Control Memory	Y - CM <sub>0</sub> (See I/O Memory)	
71 3 00 m	E7 0 m	LCM m,y	Local Control Memory	Y - CM <sub>0</sub> (See I/O Memory)	
72 0 00 m	E8 0 m	SCM m,y	Serial Control Memory	CM <sub>0</sub> -> Y (See I/O Memory)	
73 0 00 m	EC 0 0	HCR	Halt Chain	Halt chaining	
73 0 01 m	EC 1 0	IPR	Interrupt Processor	Generate chain interrupt	
73 0 00 m	EF 0 0	ZF y	Zero Flag	0 - Y, 15,14	
73 0 01 m	EF 1 0	SF y	Set Flag	1 - Y, 15,14	
74 2 00 m	F2 0 0	SMC 0,y	Serial Jump on Met Condition	Unconditional Y - CAP	
74 2 01 m	F2 1 0	SMC 1,y	Serial Jump on Met Condition	If support flag not sat, Y - CAP	
74 2 02 m	F2 2 0	SMC 2,y	Serial Jump on Met Condition	If monitor flag sat, Y - CAP	
75 0 00 m	F4 0 0	SFS m	Search For Sync	Perform functions assigned to m-bits per Page 10	
76 0 00 m	F8 0 0	CSIR m	Serial Interface Control	Set or clear discrete function per Page 10	
76 3 00 m	F8 0 3	CSST y	Serial Status	Serial Status bits - Y; See Page 10	

① a,y,m must be even

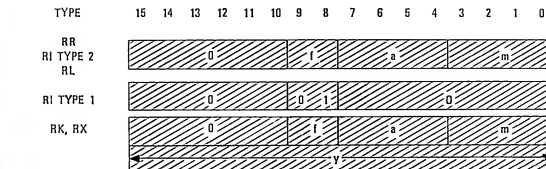
# # TRIGONOMETRIC AND HYPERBOLIC FUNCTIONS (Operation Code 37)

X, Y Cartesian coordinates. Radix point assumed to be the same  
 0 Angle of rotation Trigonometric mode (DAMS) Bit 15 = 180°  
 v Angle of rotation Hyperbolic mode Radix point assumed between bits 15 and 14  
 K 0.46872g  
 K<sub>1</sub> 1.15217g

Note: 0 results are ±1 LSB

CODING FORMAT	FUNCTION	INPUT PARAMETERS		OUTPUT RESULTS	
		R <sub>a</sub>	R <sub>a</sub> +1	Y → R <sub>a</sub>	W → R <sub>a</sub> +2
37 0 a 00	Trigonometric vector	Y	x	0	$W = \theta = \tan^{-1} \frac{Y}{X}$
37 0 a 01	Trigonometric rotate	Y	x	$\theta$	$W = \theta = \tan^{-1} \frac{Y}{X}$
37 0 a 02	Trig. vector with prescale	Y	x	0	$W = \theta = \tan^{-1} \frac{Y}{X}$
37 0 a 03	Trig. rotate with prescale	Y	x	$\theta$	$W = \theta = \tan^{-1} \frac{Y}{X}$
37 0 a 04	Hyperbolic vector	Y	x	0	$W = v = \tanh^{-1} \frac{Y}{X}$
37 0 a 05	Hyperbolic rotate	Y	x	v	0
37 0 a 06	Hyp. vector with postscale	Y	x	0	$W = v = \tanh^{-1} \frac{Y}{X}$
37 0 a 07	Hyp. rotate with postscale	Y	x	v	0
37 0 a 01	Sin $\theta$ : Cos $\theta$	0	0.46872g	$\theta$	0
37 0 a 03	Sin $\theta$ : Cos $\theta$	0	1	$\theta$	0
37 0 a 01	Polar to Cartesian without prescale	0	R	$\theta$	0
37 0 a 03	Polar to Cartesian with prescale	0	R	$\theta$	0
37 0 a 06	Log <sub>e</sub> x	x-1	x+1	0	$W = 1/2 \log_e x = \tanh^{-1} \frac{x-1}{x+1}$
37 0 a 07	Exponential	1	1	v	0

# Optional Math Pac Instructions



## DEFINITION OF FIELDS

- 0 Operation (Function) Code
- 1 Format Designator
- 00 = Format RR, Register to Register or RL-1 Format
- 01 = Format RI, Register Indirect Memory or RL-2 Format
- 10 = Format RK, Register-Literal Constant or RL-3 Format
- 11 = Format RX, Register-Indexed Address, Constant or RL-4 Format
- a General Register or Subfunction Designator
- m General Register or Subfunction Designator
- 4-bit Unsigned Literal Constant in RL Format
- 0 Signed Deviation Value (Two's Complement)
- y Address or Arithmetic Constant

## LEGEND

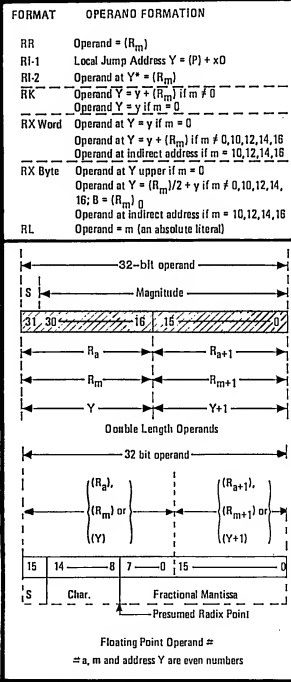
- B Byte pointer, 0 → Upper, 1 → Lower
- C Carry
- CC Condition Code
- OV Overflow
- IW Indirect Word
- J Designator Field in IW
- x General Register Designator in IW1
- y Contents of Second Instruction Word or IW2
- Y Effective Operand Address or Constant
- Y\* Effective Operand Address in R<sub>m</sub>
- TM I/O Transfer Mode
- 00 = Abort Input Transfer
- 01 = 8-bit Byte Transfer
- 10 = 16-bit Word Transfer
- 11 = 32-bit Dual Word Transfer
- BWC Buffer Word Count\*
- BAP Buffer Address Pointer
- CM Control Memory Word
- CAP Chain Address Pointer
- RTC Real-Time Clock
- ( ) Contents of register or address
- r (R<sub>a</sub>) 5-0
- r (R<sub>a</sub>) 13-8
- r (R<sub>a</sub>) 7-0
- r (R<sub>a</sub>) 15-8
- Compare
- 2's Complement

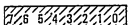
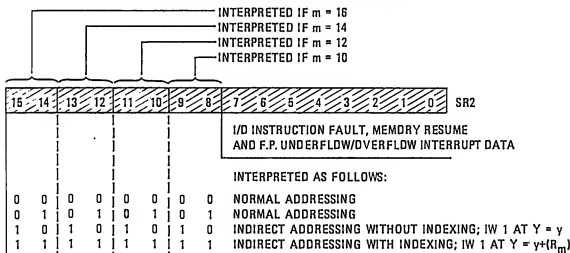
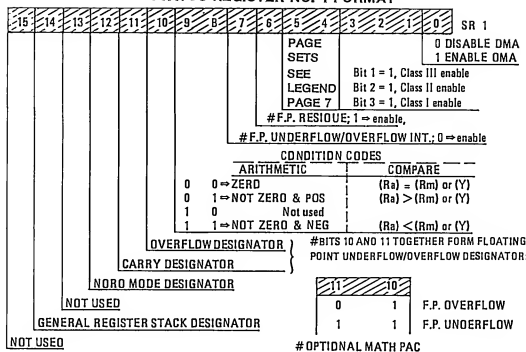
## PAGE SETS SR 1 Bits 5-4

00	Page	Set 0
01	Page	Set 1
10	Page	Set 2
11	Page	Set 3

OR	XOR	AND
V 0 1	V 0 1	A 0 1
0 0 1	0 0 1	0 0 1
1 1 1	1 1 0	1 0 1

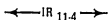
\*NOTE: If BWC = zero (0000), Indicates the maximum number of transfers (4096).





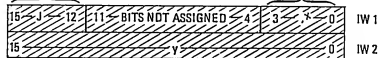
```
C C C C 0 X 1 0
0 0 0 0 0 0 0 1
1 M M M 0 0 1 0
```

CHAIN INSTRUCTION CCCC = CHAN #; X = 0 ⇒ INPUT; X = 1 ⇒ OUTPUT  
COMMAND INSTRUCTION  
MEMDRY RESUME INTERRUPT; MMM = 8K MOD. NO. (UYK-20)  
OR 32K (UYK-20A) .

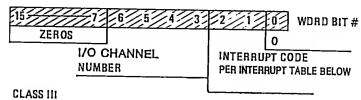
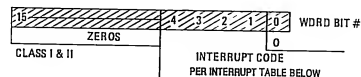


DCIAL J-VALUE	OPERAND/IWI, LOCATION
0	WORD AT Y = (IW2)
1	BYTE AT UPPER HALF OF Y = (IW2)
2	WORD AT Y = (IW2) + (R <sub>n</sub> )
3	BYTE AT Y = (IW2) + (R <sub>n</sub> ) * 2
4	WORD AT Y = (IW2) + (R <sub>m</sub> )
5	BYTE AT Y = (IW2) + (R <sub>m</sub> ) * 2
6	WORD AT Y = (IW2) + (R <sub>m</sub> + 1)
7	BYTE AT Y = (IW2) + (R <sub>m</sub> + 1) * 2
8	NEXT IW1 AT ADDRESS Y = (IW2)
9	NEXT IW1 AT ADDRESS Y = (IW2) + (R <sub>n</sub> )
10	NEXT IW1 AT ADDRESS Y = (IW2) + (R <sub>m</sub> )
11	NEXT IW1 AT ADDRESS Y = (IW2) + (R <sub>m</sub> + 1)
10-17	NOT ASSIGNED

SPECIFIES GENERAL REGISTER R<sub>n</sub> -



\* B = LSB of register

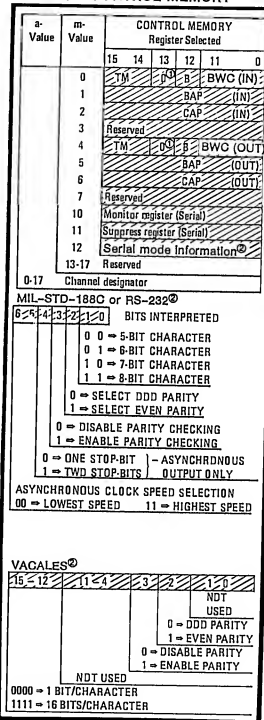


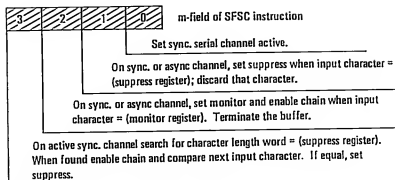
Function	Address Assignment to Class		
	III	II	I
Store P addresses	110	120	130
Store SR #1 addresses	111	121	131
Store SR #2 addresses	112	122	132
Store RTC lower addresses	113	123	133
P Reload addresses	114	124	134
SR #1 Reload addresses	115	125	135
SR #2 Reload addresses	116	126	136
Store RTC upper addresses	117	127	137
I/O Command cells	140-141		
Auto start entrance	177		
External interrupt word storage	200-217		
NDRO	00-77, 300-477		

Class	Priority Within Class	Interrupt	Binary Interrupt Code Generation
Class I, Hardware Errors	1	Power Fault	0000
	2	Memory Resume	0001
Class II, Software Interrupts	1	CP Instruction Fault	0000
	2	I/O Instruction Fault	0001
	3	F.P. Overflow/Underflow	0010
	4	* Interrupt	0011
	5	RTIC DverFlow	0100
Class III, IDC Interrupts	6	Monitor Clock	0101
	7	Write Protect (20A Only)	1100
	2	Interrupter Time-Out	00
	3	External Interrupt or Discrete Interrupt *	11
	4	Input Chain Interrupt	01
		Output Chain Interrupt	10

\* Serial MIL-STD-188C, VACALES, or EIA-STD-RS-232C  
Channels # Optional Math Pac function

<u>CM<sub>2</sub>13</u>	<u>CHANNEL NUMBER</u>	<u>PAGE SET</u>
0	N/A	00
1	0 - 7 <sub>8</sub>	10
1	10 - 17 <sub>8</sub>	11





Bits 2 and 3 used for VACALES "Search for Sync"

## SERIAL CHANNEL INTERRUPT WORD FORMAT

BITS	MIL-STO-188	RS-232	VACALES
0-7	ALWAYS ONES	ALWAYS ONES	ALWAYS ONES
8	1 = B DISCRETE TURNED ON	1 = RING INDICATOR ON	1 = B DISCRETE TURNED ON
9	1 = C DISCRETE TURNED OFF	1 = RECEIVED LINE SIGNAL DETECTOR OFF	1 = CARRIER DETECT TURNED OFF
10	1 = I DISCRETE TURNED ON	1 = I DISCRETE TURNED ON	1 = ALARM INDICATE TURNED ON
11	ALWAYS ONE	ALWAYS ONE	1 = SYNC ERROR TURNED ON
12	ALWAYS ONE	ALWAYS ONE	1 = TRANSMIT FULL ON TURNED OFF
13-15	ALWAYS ONES	ALWAYS ONES	ALWAYS ONES

## SERIAL I/O DISCRETE FUNCTIONS

Octal m-Value	Function	MIL-STO-188C/VACALES		EIA-STO-RS232	
		Discrete	Line Designator (188C)	Discrete	Line Designator
0	Set	Loop test (internal)	-	Loop test (internal)	-
1	Clear	Loop test (internal)	-	Loop test (internal)	-
2	NoOp	Not used	-	Spare	-
3	NoOp	Not used	-	Spare	-
4	Set	Control Line 6	J	J (nonstd.)	-
5	Clear	Control Line 6	J	J (nonstd.)	-
6	Set	Control Line 5	H	TRAN. PREP	-
7	Clear	Control Line 5	H	TRAN. PREP	-
10	Clear	Control Line 4	G	G	CA
11	Set	Control Line 4	G	G	CA
12	Clear	Control Line 3	F	F	New Sync
13	Set	Control Line 3	F	F	New Sync
14	Clear	Control Line 2	O	O	Out Terminal Ready
15	Set	Control Line 2	O	O	Out Terminal Ready
16	Clear	Control Line 1	A	LOOP BACK	CO
17	Set	Control Line 1	A	LOOP BACK	CO

## SERIAL I/O STATUS INTERPRETATION

Word Bit #	MIL-STO-188 Function	EIA-STO-RS232 Function	VACALES FUNCTION
2 <sup>0</sup>	Parity Error	Parity Error	-
2 <sup>1</sup>	Overrun	Overrun	Overrun
2 <sup>2</sup>	Break	Break	Parity Error
2 <sup>3</sup>	E Active	Clear to Send	Sync Error

UNIT NAME	DESIGNATION	PART NUMBER
CABINET, ELECTRICAL EQUIPMENT <sup>2</sup>	CY-7445A/UYK-20(V)	90536-7 101970-12
CABINET, ELECTRICAL EQUIPMENT <sup>3</sup>	CY-7446A/UYK-20X(V)	90536-7 101970-13
CABINET, ELECTRICAL EQUIPMENT <sup>1 3</sup>	CY-777-1/UYK-20X(V)	90536-7 157853-09
CABINET, ELECTRICAL EQUIPMENT <sup>2</sup>	CY-7976/UYK-20A(V)	90536-7 101970-14
CABINET, ELECTRICAL EQUIPMENT <sup>3</sup>	CY-7977/UYK-20AX(V)	90536-7 101970-15
CONTROL-MONITOR <sup>2</sup>	C-9674A/UYK-20(V)	90536-7 101985-10
CONTROL-MONITOR <sup>3</sup>	C-9675A/UYK-20X(V)	90536-7 101985-09
CONTROL-MONITOR <sup>1 3</sup>	C-10633/UYK-20X(V)	90536-7 157869-03
CONTROL-MONITOR <sup>2</sup>	C-9674A/UYK-20(V)	90536-7 101985-08
POWER SUPPLY <sup>2</sup>	PP-7032(V)/UYK-20(V)	90536-7 150350-02
POWER SUPPLY <sup>2</sup>	PP-7107(V)/UYK-20(V)	90536-7 150355-02
POWER SUPPLY <sup>2</sup>	PP-7108(V)/UYK-20(V)	90536-7 150351-03
POWER SUPPLY <sup>3</sup>	PP-7109(V)/UYK-20X(V)	90536-7 150352-04
POWER SUPPLY <sup>3</sup>	PP-7110(V)/UYK-20X(V)	90536-7 150354-04
POWER SUPPLY <sup>3</sup>	PP-7111(V)/UYK-20X(V)	90536-7 150353-03
PROCESSOR-VERIFIER UNIT <sup>2</sup>	CP-1188B(V)/UYK-20(V)	90536-7 128031-18
PROCESSOR-VERIFIER UNIT <sup>3</sup>	CP-1189B(V)/UYK-20X(V)	90536-7 128031-19
PROCESSOR-VERIFIER UNIT <sup>2</sup>	CP-1512(P)/UYK-20A(V)	90536-73 10550-00
PROCESSOR-VERIFIER UNIT <sup>3</sup>	CP-1513(P)/UYK-20AX(V)	90536-73 10550-01
CORE MEMORY UNIT (8K)	MU-632/UYK-20(V)	90536-7 128082-00
CORE MEMORY UNIT (32K)	MU-731/UYK-20A(V)	90536-73 10022-18
CORE MEMORY-CONTROL UNIT <sup>2</sup>	C-9531A(V)/UYK-20(V)	90536-7 128029-03
CORE MEMORY-CONTROL UNIT <sup>3</sup>	C-9570A(V)/UYK-20X(V)	90536-7 128029-21
CORE MEMORY-CONTROL UNIT <sup>2</sup>	C-9531A(V)/UYK-20(V)	90536-7 128029-22
CORE MEMORY-CONTROL UNIT <sup>3</sup>	C-9570A(V)/UYK-20X(V)	90536-7 128029-23
CORE MEMORY-CONTROL UNIT <sup>2</sup>	C-11087(V)/UYK-20A(V)	90536-73 10014-08
CORE MEMORY-CONTROL UNIT <sup>3</sup>	C-11088(V)/UYK-20AX(V)	90536-73 10014-09
INTERFACE KIT, FAST, SERIAL	MK-1720/UYK-20(V)	90536-7 101802-08
INTERFACE KIT, SERIAL COMMUNICATION		
ASYNC/SYNC MIL-188C	MK-2051/UYK-20(V)	90536-73 13567-02
INTERFACE KIT, SERIAL COMMUNICATION		
ASYNC/SYNC RS232	MK-2048/UYK-20(V)	90536-73 13568-02
INTERFACE KIT, SLOW	MK-2097/UYK-20(V)	90536-7 132194-04
INTERFACE KIT, FAST, NEGATIVE	MK-2096/UYK-20(V)	90536-7 132195-04
INTERFACE KIT, FAST, POSITIVE	MK-2099/UYK-20(V)	90536-7 132196-04
INTERFACE KIT, VARIABLE CHARACTER		
LENGTH, SERIAL (VACALES)	MK-1806/UYK-20(V)	90536-7 132198-03
INTERFACE KIT, SLOW PIC, DUAL	MK-2100/UYK-20(V)	90536-7 132197-02
INTERFACE KIT, LOW LEVEL SERIAL	MK-2130/UYK-20(V)	90536-7320276-03
MAINTENANCE KIT, ELECTRONIC		
EQUIPMENT	MK-1958/UYK-20(V)	90536-7 128073-01
REGISTER, COMPUTER, DUAL	MU-834/UYK-20(V)	90536-7 150465-01
MEMORY KIT, READ		
(AVAILABLE BOOTSTRAP LISTINGS)	MK-1901(V)/UYK-20(V)	90536-7 136820-00
ADAPTER KIT, EXTERNAL MOUNTING	MK-1959/UYK-20(V)	90536-7 157900-00
ADAPTER KIT, EXTERNAL MOUNTING	MK-1960/UYK-20(V)	90536-7 157900-01
OSCILLATOR, REAL TIME CLOCK		
MONITOR	O-1781/UYK-20(V)	90536-7 126200-02
OSCILLATOR, REAL TIME CLOCK		
MONITOR	O-1782/UYK-20(V)	90536-7 137130-02
MOUNTING KIT, INTERNAL ADAPTER	MK-2308/UYK-20(V)	90536-7321442-00

<sup>1</sup>Langley Rack    <sup>2</sup>400 Hz    <sup>3</sup>60 Hz

NOTE: For Micro Memory Items, see page 12.



## LIST OF AN/UYK-20(V) MICROMEMORY ITEMS

NAME	DESIGNATION	PART NUMBER
PROGRAM KIT, MICROMEMORY BASIC/ NO MATH PAC	MK-1723(V)/UYK-20(V)	90536-7128071-04
PROGRAM KIT, MICROMEMORY BASIC/ MATH PAC	MK-1723(V)/UYK-20(V)	90536-7128071-05
MICROMEMORY UNIT, GROWTH, PROGRAM ONE	MU-791/UYK-20(V)	90536-7136291-01
MICROMEMORY UNIT, GROWTH, PROGRAM TWO	MU-792/UYK-20(V)	90536-7136905-01
MICROMEMORY UNIT, GROWTH, PROGRAM THREE	MU-793/UYK-20(V)	90536-7137070-01
MICROMEMORY UNIT, GROWTH, PROGRAM FOUR	MU-794/UYK-20(V)	90536-7313052-01
MICROMEMORY UNIT, STANDARD	MU-799/UYK-20(V)	90536-7125133-01

## LIST OF AN/UYK-20A(V) MICROMEMORY ITEMS

NAME	DESIGNATION	PART NUMBER
PROGRAM KIT, MICROMEMORY BASIC/ NO MATH PAC	MK-2134(V)/UYK-20A(V)	90536-7310548-00
PROGRAM KIT, MICROMEMORY BASIC/MATH PAC	MK-2134(V)/UYK-20A(V)	90536-7310548-01
MICROMEMORY UNIT, GROWTH, PROGRAM I	MU-795/UYK-20A(V)	90536-7310524-01
MICROMEMORY UNIT, GROWTH, PROGRAM II	MU-796/UYK-20A(V)	90536-7310526-01
MICROMEMORY UNIT, GROWTH, PROGRAM III	MU-797/UYK-20A(V)	90536-7310538-01
MICROMEMORY UNIT, GROWTH, PROGRAM IV	MU-798/UYK-20A(V)	90536-7315270-01
MICROMEMORY UNIT, STANDARD	MU-800/UYK-20A(V)	90536-7310522-01

CARD	NAME	NSNs	LOCATION
90536-7092187-01	MICRO P REGISTER + DISPLAY	7010-01-084-8743	A03,04,05
90536-7092195-01	CONDITION REGISTER	7010-00-522-3450	B08
90536-7092201-01	REPEAT CONTROL + DISPLAY	7010-01-084-8742	A06
90536-7125129-01	MICRO MEMORY 0000-1777	7010-01-127-1757	B05*
90536-7125136-01	MICRO MEMORY 6000-7777	7010-00-522-3702	B02
90536-7125237-02	EMULATE CONTROL 1 & 2	7010-01-100-3315	C17*
90536-7125241-01	INST REG 0-7	7010-01-076-0613	C13
90536-7125276-01	MULTIPLY, DIVIDE, & MICRO CONTROL	7010-01-100-3316	B07
90536-7125290-01	SOURCE & DESTINATION TRANSLATOR	7010-00-522-3719	B15
90536-7125307-01	I/O CONTROL MEMORY	7010-01-075-5597	A20,21,22,23
90536-7125311-01	P, BKPT, MEMORY ADDRESS REG	7010-00-397-7808	C07,08
90536-7125380-01	STATUS REG 1 & 2 BITS 8-15	7010-00-522-3732	C15
90536-7125406-01	PAGE REGISTERS & CONTROL	7010-01-100-3317	C09*
90536-7125417-01	ALU CONTROL II & CONSOLE CONTROL	7010-00-578-2413	B09
90536-7125500-01	SHIFT MATRIX	7010-00-522-3735	A09,10
90536-7125926-01	PWR INTERRUPT, MASTER CLEAR	7010-00-522-3751	C22*
90536-7125980-01	I/O MODE & MATH PAC SELECT	7010-01-017-8793	C23*
90536-7126125-01	TWO BIT MULTIPLY	7010-00-522-3759	A07,08
90536-7126130-01	SHIFT MATRIX INPUT REGS.	7010-00-522-3760	A12
90536-7126156-01	MEMORY INTERFACE	7010-01-100-3318	C05,06
90536-7126160-01	RTC & MON CLK CONT, RESUME, DUAL CH	7010-00-522-3955	A14
90536-7126167-01	JUMP INTERRUPTS & INPUT ADDR	7010-01-084-8773	C19*
90536-7126172-01	I/O TRANSLATOR	7010-01-084-8785	B21
90536-7126175-01	I/O PRIORITY	7010-00-522-3987	B20
90536-7126181-01	I/O CONTROL, I/O TIMING	7010-00-522-4004	B18
90536-7126200-02	20 Mhz OSC 1 KHz CLOCK	7050-01-211-4670	B23
90536-7136266-01	ALU CONTROL	7010-01-100-3320	B10
90536-7136295-01	NDRO CONTROL PANEL INTERFACE	7010-01-006-6468	B06
90536-7136351-01	MICRO CONTROL 15	7010-01-100-3321	B17
90536-7150210-01	ARITHMETIC LOGIC UNIT	7010-01-140-7114	B11,12,13,14
90536-7150220-01	MEMORY CONTROL	7010-00-522-3749	C10*
90536-7150295-01	MASTER CLOCK, CONDITION REG	7010-00-522-3752	B16
90536-7150397-01	SHIFT MATRIX CONTROL	7010-01-053-4303	A13
90536-7150401-01	EMULATE CONTROL 3 & 4	7010-01-100-3323	C18
90536-7150405-01	TRANSLATOR CONTROL	7010-01-054-2891	B19
90536-7150415-01	STATUS REG 1 & 2 BITS 0-7	7010-01-050-1708	C16
90536-7150421-01	I/O INTERRUPT STORAGE	7010-01-100-3324	B22
90536-7150465-01	GENERAL REGISTERS (32)	5999-01-131-4654	C14
90536-7150475-01	I/O DATA DRIVE & MONITOR CLOCK	7010-01-100-3325	A19
90536-7150480-01	MICRO MEMORY SEL & MISC	7010-01-100-3326	A15

\*SEE PAGE 15 FOR AN/UYK-20A.

CURRENT LINE REPLACEABLE ASSEMBLIES (continued)

CARD	NAME	NSNs	LOCATION
	<u>I/O Options</u>		
90536-7119380-01	-3V FAST TYPE I	7010-00-522-3519	
90536-7132152-03	-3V FAST TYPE III	5998-01-126-7298	
90536-7132154-03	-3V FAST TYPE II	7010-00-522-3526	
90536-7119395-01	-15V SLOW TYPE I	7010-00-522-3529	
90536-7132150-03	-15V SLOW TYPE II	5999-01-262-3942	
90536-7132146-13	-15V SLOW TYPE III	5999-01-262-3941	
90536-7119410-01	+3.5V ANEW TYPE I	7010-00-522-3546	
90536-7132156-03	+3.5V ANEW TYPE III	7010-00-522-3554	
90536-7132158-03	+3.5V ANEW TYPE II	7010-01-168-8386	
90536-7119432-02	NTDS SERIAL 2 CHAN RCVR	7010-01-228-3269	
90536-7312344-08	NTDS SERIAL 2 CHAN DRVR	5999-01-252-1648	
90536-7132110-01	-15 VOLT SLOW PIC TYPE I	7010-01-037-9654	
90536-7132148-13	-15 VOLT SLOW PIC TYPE II	7010-01-171-4553	
90536-7132140-01	-15 VOLT SLOW PIC TYPE IA	7010-01-037-9655	
90536-7132121-03	VACALES TYPE III	7010-01-037-9658	
90536-7132126-01	VACALES TYPE IA	7010-01-150-4425	
90536-7132131-03	VACALES TYPE II	5998-01-150-4426	
90536-7132136-01	VACALES TYPE I	7010-01-037-9657	
90536-7312528-00	COMMON RS-232/188C RCVR	7010-01-168-3843	
90536-7312530-02	COMMON MIL-188C I/O DRVR	7010-01-222-2644	
90536-7312670-04	COMMON RS-232-C I/O DRVR	5999-01-263-5745	
90536-7316476-02	LOW LEVEL SERIAL TYPE I	7010-01-168-8576	
90536-7316478-07	LOW LEVEL SERIAL TYPE II	5999-01-294-2533	
	<u>CP OPTIONS</u>		
90536-7125175-01	INST REG 08-15, ECW w/MATH PAC	7010-00-522-3704	C12
90536-7126066-01	CORDIC EXTENSION w/MATH PAC	7010-01-017-8766	A18
90536-7136226-01	MULTIPLY CONTROL w/MATH PAC	7010-01-127-1758	A11
90536-7136291-01	MPG 1 MICROMEMORY 2000-3777	7010-01-084-8798	B04*
90536-7136905-01	MPG 2 MICROMEMORY 2000-3777	5998-01-179-0551	B04*
90536-7137000-01	MICROMEMORY 4000-5777 w/MATH PAC	7010-00-578-2303	B03
90536-7137070-01	MPG 3 MICROMEMORY 2000-3777	5999-01-178-8565	B04*
90536-7137130-02	20 MHz OSC, 32 KHz CLOCK	5998-01-104-7171	B23
90536-7313052-01	MPG 4 MICROMEMORY 2000-3777	5998-01-158-4757	B04*
90536-7125133-01	MICRO MEMORY 2000-3777 w/o MICRO GROWTH	7010-01-084-8787	B04*
90536-7125157-01	INST REG 08-15, ECW ROM w/o MATH PAC	7010-00-578-2302	C12
90536-7126142-01	MULTIPLY w/o MATH PAC	7010-01-127-1756	A11
	<u>CP CABLE ASSY</u>		
90536-7101963-01	CABLE ASSY CP-TO MEM W3	7010-01-037-9651	C03
90536-7101966-01	CABLE ASSY CP-TO MEM W4	7010-01-037-9652	C04
90536-7133909-01	CABLE ASSY CP-MAINT PANEL W2	7010-00-604-9079	A02
90536-7133910-02	CABLE ASSY CP-MAINT PANEL W1	7010-00-604-8858	A01
90536-7134942-00	CABLE ASSY CP-MEM INT W6 DMA	7010-01-037-9653	C01
90536-7134998-00	CABLE ASSY CP-MEM INT W7 DMA	7010-01-026-8023	C02

\*SEE PAGE 15 FOR AN/UYK-20A.

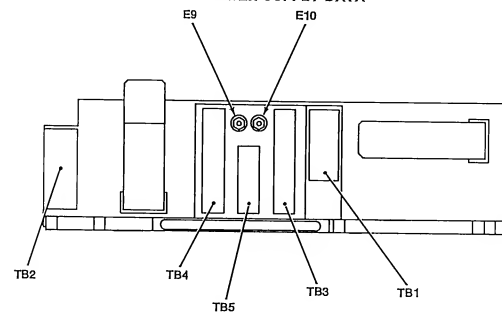
CURRENT LINE REPLACEABLE ASSEMBLIES (continued)

CARD	NAME	NSNs	LOCATION
	<u>LANGLEY RACK CP CABLE ASSY</u>		
90536-7101963-02	CABLE ASSY CP TO MEM W3	5995-01-101-5840	C03
90536-7101966-02	CABLE ASSY CP TO MEM W4	5995-01-101-5843	C04
90536-7133909-02	CABLE ASSY CP TO MAINT PNL W2	5995-01-099-2449	A02
90536-7133910-03	CABLE ASSY CP TO MAINT PNL W1	5995-01-101-5839	A01
90536-7134942-01	CABLE ASSY CP TO MEM W6 (DMA)	5995-01-062-6245	C01
90536-7134998-01	CABLE ASSY CP TO MEM W7 (DMA)	5995-01-062-6246	C02
	<u>MEMORY</u>		
90536-7128082-00	CORE ARRAY 8K	7010-01-016-0411	
90536-7150490-00	CONTROL w DMA	7010-00-525-1215	
90536-7134994-03	CONTROL w/o DMA	7010-01-084-8786	
90536-7150486-00	DATA w DMA	7010-01-066-7586	
90536-7101824-03	DATA w/o DMA	7010-01-084-8774	
	<u>EXPANDED MEMORY CP CARDS</u>		
90536-7310510-02	EMULATE CONTROL 1 & 2	7010-01-201-7389	C17
90536-7310512-01	I/O MODE & MATH PACK SEL	7010-01-201-7390	C23
90536-7310514-01	OC=40 JUMPS, INT'S, INPUT ADD REG	7010-01-201-7391	C19
90536-7310516-02	MEMORY CONTROL	5998-01-207-6600	C10
90536-7310518-01	PAGE REG'S & CONTROL	7010-01-201-7393	C09
90536-7310520-01	MICROMEMORY 0000-1777	7010-01-172-0807	B05
90536-7310522-01	MICROMEMORY 2000-3777	7010-01-181-3856	B04
90536-7310524-01	MPG 1 MICROMEMORY 2000-3777	7010-01-181-3857	B04
90536-7310526-01	MPG 2 MICROMEMORY 2000-3777	7010-01-172-9028	B04
90536-7310534-05	LOGIC CARD 1	5999-01-210-8963	C20
90536-7310536-03	POWER INT & MASTER CLEAR	7010-01-201-7395	C22
90536-7310538-01	MPG 3 MICROMEMORY 2000-3777	7010-01-172-5911	B04
90536-7315270-01	MPG 4 MICROMEMORY 2000-3777	7010-01-172-9029	B04
	<u>EXPANDED MEMORY CARDS</u>		
90536-7310022-18	CORE ARRAY 32K	7010-01-168-8583	
90536-7313550-13	DATA MOD	7010-01-167-2555	
90536-7312682-07	CONTROL CARD	7010-01-167-2554	
	<u>FAN ASSEMBLIES</u>		
90536-7309623-00	400 Hz STD CABINET	4140-01-181-8745	
90536-7309623-01	60 Hz STD CABINET	4140-01-130-0472	
90536-7310594-01	60 Hz CABINET (LANGLEY RACK)	7010-01-181-3307	
90536-7308013-00	400 Hz MEMORY	4140-01-008-2026	
90536-7308013-01	60 Hz MEMORY	4140-01-037-9620	
90536-7308028-00	400 Hz CP/O	4140-01-034-7819	
90536-7308028-01	60 Hz CP/O	4140-01-130-0471	
	<u>POWER SUPPLIES</u>		
90536-7150350-02	400 Hz, 115 VAC, 30	7010-01-016-0413	
90536-7150351-03	400 Hz, 115 VAC, 10	6130-01-130-8050	
90536-7150352-04	60 Hz, 115 VAC, 30	7010-01-125-2309	
90536-7150353-03	60 Hz, 115 VAC, 10	6130-01-129-5997	
90536-7150354-04	60 Hz, 208 VAC, 30	7010-01-164-9955	
90536-7150355-02	400 Hz, 208 VAC, 30	6130-01-130-8051	



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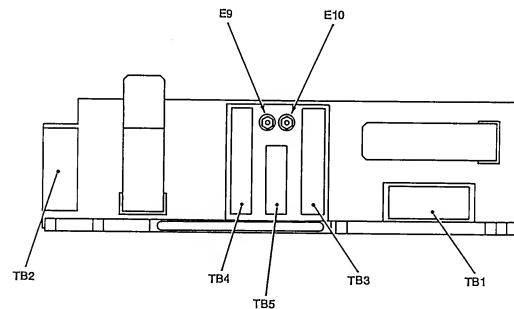
### POWER SUPPLY DATA



FRONT

POWER SUPPLY CHASSIS FOR:

PP-7109(V)/UYK-20X(V) (60 HZ 115 VAC 3Ø) 90536-7150352-04, NSN 7010-01-125-2309  
PP-7110(V)/UYK-20X(V) (60 HZ 208 VAC 3Ø) 90536-7150354-04, NSN 7010-01-164-9955



FRONT

POWER SUPPLY CHASSIS FOR:

PP-7032(V)/UYK-20(V) (400 HZ 115 VAC 3Ø) 90536-7150350-02, NSN 7010-01-016-0413  
PP-7107(V)/UYK-20(V) (400 HZ 208 VAC 3Ø) 90536-7150355-02, NSN 6130-01-130-8051  
PP-7108(V)/UYK-20(V) (400 HZ 115 VAC 1Ø) 90536-7150351-03, NSN 6130-01-130-8050  
PP-7111(V)/UYK-20X(V) (60 HZ 115 VAC 1Ø) 90536-7150353-03, NSN 6130-01-129-8997

### LOGIC VOLTAGES

OUTPUT POWER	VOLTAGE LIMITS (VDC)		LOAD CURRENT (AMPERES)		TESTPOINT
	MIN.	MAX.	MIN.	MAX.	
+5 VDC (OP/IOC)	4.8	5.4	30	42	PS1-E9
+5 VDC (MEMORY)	4.75	5.5	6	16	PS1-TB4-6
+15 VDC*	14.1	16.4	1	12	PS1-TB4-2
-5.2 VDC	-4.9	-5.6	2	10	PS1-TB3-1
+12 VDC	11.2	12.6	1	3	PS1-TB3-3
-16 VDC	-15	-16.8	0	3	PS1-TB3-5

Check all voltages between TP listed and E10.

\*The +15 volt regulator is temperature compensating and the +15 volt output will vary linearly with temperature from approximately 14.1 V at 60°C to 16.4 V at 0°C (for UYK-20A the range is 16.1 V at 60°C to 16.7 V at 0°C). Check all voltages between TP listed and E10.

## AC AND DC TEST PROCEDURES

### WARNING

FAILURE TO disconnect power cable at J35 results in dangerous voltages within the cabinet.

1. Ensure DPS main power cable is disconnected at J35.
2. Ensure all logic modules and 64K memory are installed.
3. Set Control Panel switches to the following positions:

POWER BLOWER	ON/OFF	to ON
POWER LOGIC	ON/OFF	to ON
CIRCUIT BREAKER	ON/OFF	to ON
BATTLE SHORT	ON/OFF	to ON

4. Using a VOM, observe reading as specified in the following table. Record all reading for future reference.
5. Using a VOM, measure from each power supply output voltage terminal to all other output voltage terminals. Observe the following:
  - a) TB3-1 to TB4-4 is less than 1 ohm.
  - b) All other readings are greater than 4 ohms.

### AC-DC RESISTANCE VALUES

TERMINALS		115 V 1φ		115 V 3φ		208 V 3φ	
FROM	TO	60 Hz	400 Hz	60 Hz	400 Hz	60 Hz	400 Hz
J35-A	GND STUD	> 20k	> 20k	> 20k	> 20k	> 20k	> 20k
J35-B	GND STUD	> 20k	> 20k	> 20k	> 20k	> 20k	> 20k
J35-C	GND STUD	> 20k	> 20k	> 20k	> 20k	> 20k	> 20k
J35-D	GND STUD	> 20k	> 20k	> 20k	> 20k	> 20k	> 20k
J35-G	GND STUD	< 1	< 1	< 1	< 1	< 1	< 1
J35-A	J35-B	> 30	> 15	> 100	> 30	> 200	> 90
J35-A	J35-C	> 30	> 20k	> 60	> 20	> 200	> 100
J35-A	J35-D	> 20k	> 20k	> 20k	> 20k	> 100	> 50
J35-B	J35-C	> 1	> 20k	> 150	> 60	> 200	> 90
J35-B	J35-D	> 20k	> 20k	> 20k	> 80	> 30	> 30
J35-C	J35-D	> 20k	> 1	> 20k	> 20k	> 100	> 50
P.S. TB4-6	P.S. E10	> 2	> 2	> 2	> 2	> 2	> 2
P.S. TB4-4	P.S. E10	> 2	> 2	> 2	> 2	> 2	> 2
P.S. TB4-3	P.S. E10	> 2	> 2	> 2	> 2	> 2	> 2
P.S. TB4-2	P.S. E10	> 2	> 2	> 2	> 2	> 2	> 2
P.S. E09	P.S. E10	> 1	> 1	> 1	> 1	> 1	> 1
P.S. TB3-1	P.S. E10	> 2	> 2	> 2	> 2	> 2	> 2
P.S. TB3-3	P.S. E10	> 2	> 2	> 2	> 2	> 2	> 2
P.S. TB3-5	P.S. E10	> 2	> 2	> 2	> 2	> 2	> 2
P.S. TB5-2	P.S. E10	> 2	> 2	> 2	> 2	> 2	> 2
P.S. TB4-5	P.S. E10	< 1	< 1	< 1	< 1	< 1	< 1
P.S. TB4-7	P.S. E10	< 1	< 1	< 1	< 1	< 1	< 1
P.S. TB5-3	P.S. E10	< 1	< 1	< 1	< 1	< 1	< 1
CPU TB1-6	MEM TB1-3	< 1	< 1	< 1	< 1	< 1	< 1
CPU TB1-7	MEM TB1-4	< 1	< 1	< 1	< 1	< 1	< 1
CPU TB1-6	P.S. TB2-2	< 1	< 1	< 1	< 1	< 1	< 1
CPU TB1-7	P.S. TB2-1	< 1	< 1	< 1	< 1	< 1	< 1

## I/O CONNECTOR PANEL

### INPUT/OUTPUT CONNECTOR MATING KITS J01 THRU J32

90536-7101943-02 (INPUT), NSN 5935-01-023-1213 } PARALLEL  
-03 (OUTPUT), NSN 5935-01-023-1214 } 2U45 CABLE

90536-7101943-12 (INPUT), NSN 5935-01-108-3946 } PARALLEL  
-13 (OUTPUT), NSN 5935-01-108-3945 } 2U19 CABLE

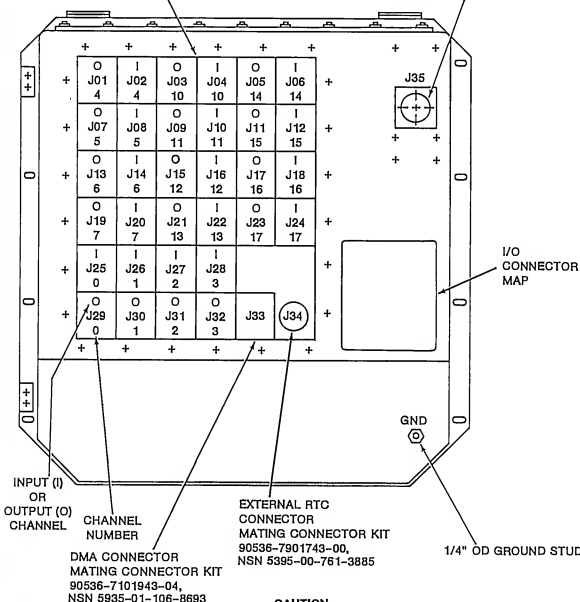
The 05 kit is used for the 188C and VACALES serial I/O. The 06 kit is used for the RS232 serial I/O.

90536-7101943-17 INPUT } PARALLEL  
-18 OUTPUT } 2U-30 CABLE

90536-7316994-00 ADAPTER } INPUT PARALLEL OR  
90536-7150267-00 MATING KIT } COMMON SERIAL

90536-7316994-01 ADAPTER } OUTPUT PARALLEL OR  
90536-7150267-01 MATING KIT } COMMON SERIAL

INPUT POWER CONNECTOR  
MATING CONNECTOR KITS  
90536-7150314-00 400 Hz,  
NSN 7010-01-100-3221  
90536-7150314-01 60 Hz,  
NSN 5935-01-106-1520



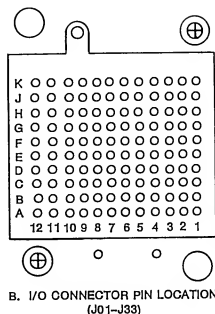
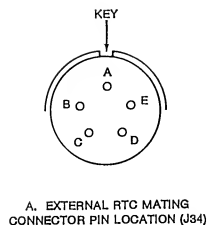
### CAUTION

CONNECTOR CAPS WITH GASKETS MUST BE INSTALLED ON UNUSED CONNECTORS TO MAINTAIN RFI/EMI INTEGRITY.

I/O CONNECTOR GASKET - P/N 90536-7101924-00, NSN 5999-01-160-7904  
CONNECTOR CAP KIT P/N 90536-7150304-00, NSN 7010-01-100-3220  
RTC CAP P/N 90536-7908845-00, NSN 0099-LL-MC2-2617

CABINET CONNECTORS (J1 THRU J33) ARE ASSEMBLED WITH INDIVIDUALLY REPLACEABLE PINS AND BUSHINGS THAT ARE FIELD REPAIRABLE. SEE TECHNICAL MANUAL FOR PROCEDURE.  
PIN/BUSHING P/N IS 90536 - 7902836-01. NSN 5940-00-516-1702  
PIN P/N IS 90536-7076100-02 NSN 5999-00-005-3847  
BUSHING P/N IS 90536-7050017-00 NSN 5999-00-003-8209

# RTC AND I/O CONNECTOR PIN LOCATION



## EXTERNAL REAL-TIME CLOCK CONNECTOR (J34) PIN ASSIGNMENTS

(MATING CONNECTOR KIT 90536-7901743-00), NSN 5935-00-761-3885  
(RECOMMENDED CABLE 90536-7128045-00)  
(RFI/EMI RTC PROTECTIVE CAP: 90536-7908845-00)

FUNCTION	CONNECTOR PIN
SPARE	A
SPARE	B
CLOCK SIGNAL RETURN	C
CLOCK SIGNAL	D
SPARE	E
SPARE	F

## SERIAL CONNECTOR PIN ASSIGNMENTS

NTDS SERIAL TYPE D CONNECTOR KITS  
(WITHOUT MATING CONNECTORS)

RG11; INPUT 90536-7150391-00, NSN 5935-01-161-2976,  
OUTPUT 90536-7150391-01, NSN 5935-01-161-2977  
RG12; INPUT 90536-7150391-02, NSN 5935-01-161-2978,  
OUTPUT 90536-7150391-03, NSN 5935-01-161-2979

NATO SERIAL TYPE E LOW LEVEL CONNECTOR KITS  
(WITHOUT MATING CONNECTORS)

TRF8; INPUT 90536-7320185-00, OUTPUT 90536-7320185-01  
TRF58; INPUT 90536-7320185-00, OUTPUT 90536-7320185-01

SIGNAL	RETURN
B 08	A 08

## MIL-STD-188C, VACALES, AND RS-232C SERIAL CHANNEL I/O CONNECTOR PIN ASSIGNMENTS

MATING CONNECTOR KITS 90536-7101943-05, NSN 5935-01-090-4460, MIL-STD-188 AND VACALES, AND 90536-7101943-06, NSN 5935-01-171-3650, RS-232

NOTE: SERIAL I/O JUMPER PLUG 90536-7150233-00, NSN 5935-01-089-5459 REQUIRED FOR END-AROUND TESTING

FUNCTION			CONNECTOR PIN	
MIL-STD-188C	RS-232C	VACALES	GROUP A*	GROUP B**
A	LOOP TEST	LOOP BACK	D-8	G-4
B	RING INDICATOR	B	D-4	D-12
C	RECEIVED LINE SIGNAL DETECTOR	CARRIER DETECT	C-4	C-12
D	DATA TERMINAL READY	D	C-8	H-4
E	CLEAR TO SEND	SYNC ERROR	D-5	G-1
F	NEW SYNC.	F	D-7	G-3
G	REQUEST TO SEND	G	C-7	H-3
H	-	TRANSMITTER PREP	D-6	G-2
I	I (NOT USED)	ALARM INDICATE	D-3	D-11
J	J (NOT USED)	J	C-6	H-2
K	DATA SET READY	RECEIVER FULL ON	C-3	C-11
L	TRANSMITTER ON FULL (NOT USED)	TRANSMITTER FULL ON	D-2	D-10
TRANSMIT CLOCK	TRANSMITTER SIGNAL	TRANSMIT CLOCK	B-5	
TRANSMIT DATA	TRANSMITTED DATA	TRANSMIT DATA	A-5	
RECEIVE CLOCK	RECEIVER SIGNAL	RECEIVE DATA	A-7	
RECEIVE DATA	ELEMENT TIMING	CLOCK	B-7	
	RECEIVE DATA	DATA SIGNAL GROUND	A-6	

NOTE: REMAINING PINS NOT USED. GROUP A OR B PINS MAY BE CONNECTED INTERNAL TO THE CABLE CONNECTOR TO ALLOW ITS USE ON EITHER A OR B GROUPS. FUNCTION TO PIN RELATIONSHIP REMAINS THE SAME FOR COMMON SERIAL I/O.

\* GROUP A: CHANNELS 0, 1; 4, 5; 10, 11; AND 14, 15 (OCTAL)

\*\* GROUP B: CHANNELS 2, 3; 6, 7; 12, 13; AND 16, 17 (OCTAL)

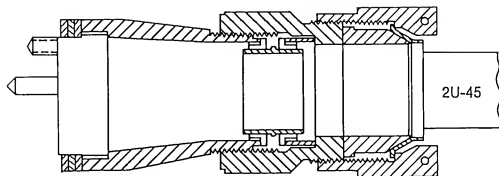
## DIRECT MEMORY ACCESS CONNECTOR (J33) PIN ASSIGNMENTS

MATING CONNECTOR KIT 90536-7101943-04, NSN 5935-01-160-8693

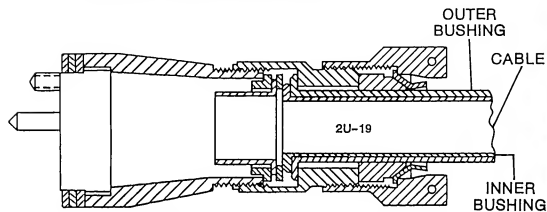
FUNCTION		CONNECTOR PIN		FUNCTION		CONNECTOR PIN	
SIGNAL	RETURN	SIGNAL	RETURN	SIGNAL	RETURN	SIGNAL	RETURN
READ INITIATE	K-8	K-7	DATA BIT 00	K-2	K-1		
WRITE INITIATE	J-8	J-7	DATA BIT 01	J-2	J-1		
FULL CYCLE	H-8	H-7	DATA BIT 02	H-2	H-1		
DATA AVAILABLE	G-8	G-7	DATA BIT 03	G-2	G-1		
ADDRESS BIT 00	F-8	F-7	DATA BIT 04	F-2	F-1		
ADDRESS BIT 01	E-8	E-7	DATA BIT 05	E-2	E-1		
ADDRESS BIT 02	D-8	D-7	DATA BIT 06	D-2	D-1		
ADDRESS BIT 03	C-8	C-7	DATA BIT 07	C-2	C-1		
ADDRESS BIT 04	B-8	B-7	*ADDR BIT 16	B-5	B-4		
ADDRESS BIT 05	A-8	A-7	ZWL	A-2	A-1		
ADDRESS BIT 06	K-11	K-10		C-12	C-11		
ADDRESS BIT 07	J-11	J-10	DATA BIT 08	K-5	K-4		
ADDRESS BIT 08	H-11	H-10	DATA BIT 09	J-5	J-4		
ADDRESS BIT 09	G-11	G-10	DATA BIT 10	H-5	H-4		
ADDRESS BIT 10	F-11	F-10	DATA BIT 11	G-5	G-4		
ADDRESS BIT 11	E-11	E-10	DATA BIT 12	F-5	F-4		
ADDRESS BIT 12	D-11	D-10	DATA BIT 13	E-5	E-4		
ADDRESS BIT 13	C-11	C-10	DATA BIT 14	D-5	D-4		
ADDRESS BIT 14	B-11	B-10	DATA BIT 15	C-5	C-4		
ADDRESS BIT 15	A-11	A-10	*ADDR BIT 17	B-2	B-1		
			ZWU	A-5	A-4		

Note: Remaining pins not used.

\*AN/UYK-20A only



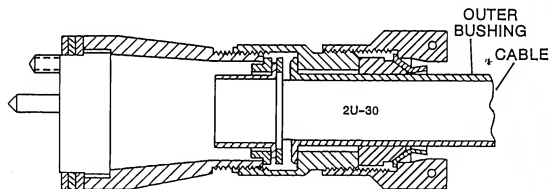
90536-7101943-02 (INPUT) NSN 5935-01-023-1213  
90536-7101943-03 (OUTPUT) NSN 5935-01-023-1214  
CONNECTOR STANDARD PARALLEL



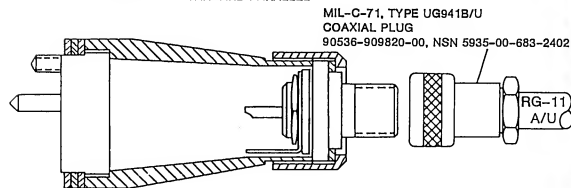
90536-7101943\*-12 (INPUT) NSN 5935-01-108-3946  
90536-7101943\*-13 (OUTPUT) NSN 5935-01-108-3945  
CONNECTOR STANDARD PARALLEL

\*SAME KIT IS USED FOR 8-BIT PARALLEL  
USING 2U-19 CABLE AND BOTH BUSHINGS

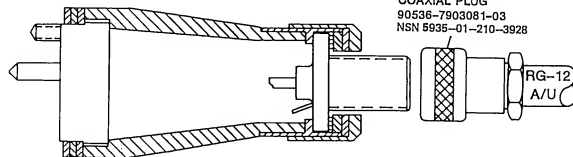
THE MIL-STD-188C AND VAGALES CONNECTOR KIT 90536-7101943-05, NSN 5935-01-090-4460  
AND RS-232C CONNECTOR KIT 90536-7101943-06, NSN 5935-01-171-3650  
ARE SIMILAR TO THE PARALLEL 2U-19 KITS AND CAN BE USED WITH ANY MULTIWIRED CABLE.



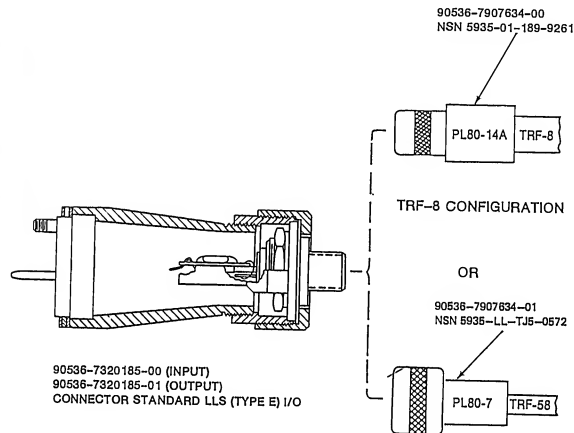
90536-7101943-17 (INPUT)  
90536-7101943-18 (OUTPUT)  
CONNECTOR STANDARD PARALLEL



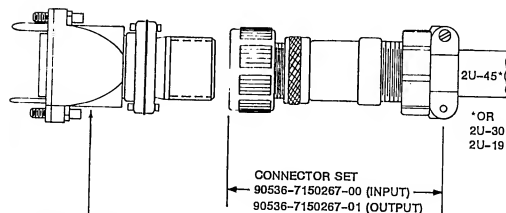
90536-7150391-00 (INPUT) NSN 5935-01-161-2976  
90536-7150391-01 (OUTPUT) NSN 5935-01-161-2977  
CONNECTOR STANDARD NTDS SERIAL (TYPE D) RG-11 CONFIGURATION



90536-7150391-02 (INPUT) NSN 5935-01-161-2978  
90536-7150391-03 (OUTPUT) NSN 5935-01-161-2979  
CONNECTOR STANDARD NTDS SERIAL (TYPE D) RG-12 CONFIGURATION



TRF-58 CONFIGURATION



90536-7316994-00 INPUT  
90536-7316994-01 OUTPUT  
MIL-C-38999 SERIES III  
CONNECTOR ADAPTER

CONNECTOR SET  
90536-7150267-00 (INPUT)  
90536-7150267-01 (OUTPUT)

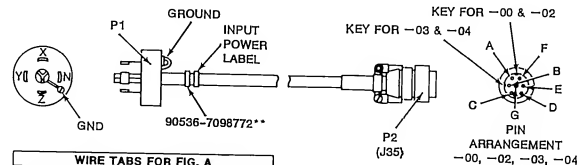
# I/O CONNECTOR TYPE PIN TO PIN CROSS REFERENCE DATA

INPUT	MIL-C-38999 79 PIN	120 PIN	90 PIN	85 PIN	OUTPUT
IDR	79-78	B5-A5	1-11	1-6	ODA
IDA	77-76	B6-A6	2-12	2-7	ODR
EIR	75-74	B7-A7	3-13	3-8	EFA
EIA	73-72	B8-A8	4-14	4-9	EFR
DATA BIT 0	71-70	D1-C1	5-15	5-21	DATA BIT 0
DATA BIT 1	69-68	D2-C2	10-20	14-22	DATA BIT 1
DATA BIT 2	67-66	D3-C3	22-33	15-23	DATA BIT 2
DATA BIT 3	65-64	D4-C4	23-34	16-24	DATA BIT 3
DATA BIT 4	63-62	D5-C5	24-35	17-25	DATA BIT 4
DATA BIT 5	61-60	D6-C6	25-36	18-26	DATA BIT 5
DATA BIT 6	59-58	D7-C7	26-37	29-39	DATA BIT 6
DATA BIT 7	57-56	D8-C8	27-38	30-40	DATA BIT 7
DATA BIT 8	55-54	D9-C9	28-39	31-41	DATA BIT 8
DATA BIT 9	53-52	D10-C10	29-40	32-42	DATA BIT 9
DATA BIT 10	51-50	D11-C11	30-41	33-43	DATA BIT 10
DATA BIT 11	49-48	D12-C12	31-42	34-44	DATA BIT 11
DATA BIT 12	47-46	G1-H1	32-43	35-45	DATA BIT 12
DATA BIT 13	45-44	G2-H2	47-58	36-46	DATA BIT 13
DATA BIT 14	43-42	G3-H3	48-59	37-47	DATA BIT 14
DATA BIT 15	41-40	G4-H4	49-60	49-58	DATA BIT 15
DATA BIT 16	39-38	G5-H5	50-61	50-59	DATA BIT 16
DATA BIT 17	37-36	G6-H6	51-62	51-60	DATA BIT 17
DATA BIT 18	35-34	G7-H7	52-63	52-61	DATA BIT 18
DATA BIT 19	33-32	G8-H8	53-64	53-62	DATA BIT 19
DATA BIT 20	31-30	G9-H9	54-65	54-63	DATA BIT 20
DATA BIT 21	29-28	G10-H10	55-66	55-64	DATA BIT 21
DATA BIT 22	27-26	G11-H11	56-67	56-65	DATA BIT 22
DATA BIT 23	25-24	G12-H12	57-68	57-66	DATA BIT 23
DATA BIT 24	23-22	J1-K1	70-80	67-75	DATA BIT 24
DATA BIT 25	21-20	J2-K2	71-81	68-76	DATA BIT 25
DATA BIT 26	19-18	J3-K3	72-82	69-77	DATA BIT 26
DATA BIT 27	17-16	J4-K4	73-83	70-78	DATA BIT 27
DATA BIT 28	15-14	J5-K5	74-84	71-79	DATA BIT 28
DATA BIT 29	13-12	J6-K6	75-85	72-80	DATA BIT 29
DATA BIT 30	11-10	J7-K7	76-86	73-81	DATA BIT 30
DATA BIT 31	9-8	J8-K8	77-87	5-12	DATA BIT 31
DATA BIT 32		J9-K9	5-15	10-11	DATA BIT 32
DATA BIT 33		J10-K10	6-16	82-83	DATA BIT 33
DATA BIT 34		J11-K11	7-17	19-27	DATA BIT 34
DATA BIT 35		J12-K12	8-18	84-85	DATA BIT 35
SPARE	5-6	B2-A2	21-46	28-20	SPARE
SPARE	3-4	B3-A3	44-79	38-48	SPARE
SPARE	1-2	B4-A4			SPARE
SPARE		B9-A9			SPARE
SPARE		B10-A10			SPARE
SHIELD	7	B1	45-69	74	SHIELD

NOTE: FOR ARMORED CABLE THE SHIELD IS TO BE CONNECTED TO THE APPROPRIATE PIN IN THE CONNECTOR BLOCK.

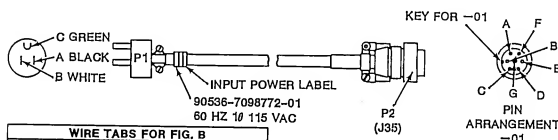
IN COLUMNS LISTING PIN NUMBERS THE FIRST PIN LISTED CARRIES THE ACTIVE SIGNAL AND THE SECOND THE RETURN.

## POWER CONNECTOR DATA

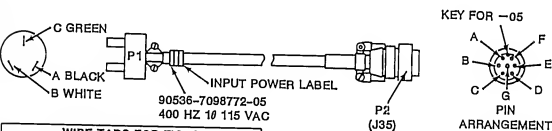


ORIGIN	WIRE COLOR	DESTINATION
P1-X	BLACK	P2-A
P1-Y	RED	P2-B
P1-Z	ORANGE	P2-C
P1-N	WHITE	P2-D
P1-GND	GREEN	P2-G

-00 400 HZ 3Ø 115 VAC  
-02 400 HZ 3Ø 208 VAC  
-03 60 HZ 3Ø 115 VAC  
-04 60 HZ 3Ø 208 VAC



ORIGIN	WIRE COLOR	DESTINATION
P1-A	BLACK	P2-A
P1-B	WHITE	P2-B
P1-C	GREEN	P2-G



ORIGIN	WIRE COLOR	DESTINATION
P1-A	BLACK	P2-A
P1-B	WHITE	P2-B
P1-C	GREEN	P2-G

POWER CONNECTOR (J35) PIN ASSIGNMENTS:  
MATING CONNECTOR KITS: 90536-7150314-00, 400 Hz; MS 9106R20-15S, NSN 7010-01-100-3221  
90536-7150314-01, 60 Hz; MS 3106R20-15SZ, NSN 5935-01-106-1520

PIN NO.	1 Ø	3 ØY (208V)	3 ØΔ
A	115 VAC	115 VAC LINE TO NEUTRAL (Ø A)	115 VAC LINE TO LINE (Ø A)
B	NEUTRAL (COMMON)	115 NEUTRAL LINE TO NEUTRAL (Ø B)	115 VAC LINE TO LINE (Ø B)
C	NOT USED	115 VAC LINE TO NEUTRAL (Ø C)	115 VAC LINE TO LINE (Ø C)
D	NOT USED	NEUTRAL (COMMON)	NOT USED
E	NOT USED	NOT USED	NOT USED
F	NOT USED	NOT USED	NOT USED
G	SAFETY GROUND	SAFETY GROUND	SAFETY GROUND



# AVAILABLE NDRO PROGRAM KIT CONFIGURATIONS

This list contains the available NDRO Program Kit configurations. These bootstraps were developed for AN/UYK-20 users and are under AN/UYK-20 Baseline Control. Other bootstraps developed by Unlsys for non-military use are listed under Unlsys engineering drawing 7137880. A bootstrap list cross referenced by device is available from A. L. Edwins (612) 456-7411 or write to:

Unlsys Corporation  
Defense Products  
P.O. Box 64525  
St. Paul Mn. 55164-0525  
Attn: A. L. Edwins Software Products  
M.S. Y42B1.

## BOOTSTRAPS DEVELOPED FOR AN/UYK-20(V) AND AN/UYK-20A(V) COMPUTERS

PART NUMBER	BOOT NAME DEVICE-1 NAME DEVICE-2 NAME	OCTAL CHAN NO	BOOT STRAP SWITCH	PX10563 SEC. NO.
90536-7125150	EWDR PERTEC MTU 556 BPI REMEX 6375 PAPER TAPE	CHAN 07 CHAN 04	1 2	3-1
90536-7136150	CVTSC UNIVAC 1840M MTU INTERCOMPUTER	CHAN 01 CHAN 00-04	1 2	3-2
90536-7136155	SYS-1 UNIVAC 1540 MTU UNIVAC 1532 PAPER TAPE	CHAN 17 CHAN 16	1 2	3-3
90536-7136160	JOIC UNIVAC 1540 MTU INTERCOMPUTER	CHAN 00 CHAN 03-07	1 2	3-4
90536-7136165	ESMDE UNIVAC 1540 MTU UNIVAC 1532 PAPER TAPE	CHAN 01 CHAN 00	1 2	3-5
90536-7136170	STANDARD UNIVAC 1540 MTU UNIVAC 1532 PAPER TAPE	CHAN 00 CHAN 01	1 2	3-6
90536-7136186	SSIXS(A) CIPHER MARK I MTU SYSTEM INDUST. 3500-33 DISK	CHAN 15 CHAN 17	1 2	3-7
90536-7136190	SSIXS(B) CIPHER DATA PRO. C-200 CASS. REMEX 6375 PAPER TAPE	CHAN 00 CHAN 01	1 2	3-8
90536-7136195	OW-75(A) UNIVAC 1840M MTU UNIVAC 1538 PAPER TAPE	CHAN 03 CHAN 02	1 2	3-19
90536-7136205	SAMAC KENNEDY 9000 MTU EECO PAPER TAPE	CHAN 11 CHAN 07	1 2	3-11
90536-7136210	SSQ-72 DIGITRONICS 2540 PTR	CHAN 10	1-2	3-12
90536-7136216	TPN22 KENNEDY 9000 MTU	CHAN 03	1-2	3-27

# AVAILABLE NDRO PROGRAM KIT CONFIGURATIONS (continued)

90536-7136220	90536-7136230	90536-7136235	90536-7136245	90536-7136250	90536-7136256	90536-7136260	90536-7136270	90536-7136275	90536-7136281	90536-7136305	90536-7136310	90536-7136315	90536-7136320	90536-7136325	90536-7136330
CFP UNIVAC 1532 PAPER TAPE	GARD N.A.F.I PAPER TAPE TT-187,5-LEVEL PTPRDR	ADSCS O-172 DEAC MTU KENNEDY 9000 MTU	SSS(A) UNIVAC 1840M MTU UNIVAC 1532 PAPER TAPE	SSS(B) KENNEDY 9000 MTU UNIVAC 1004 CARD RDR	MK-48 UNIVAC 1544 MTU 601 CARD READER	E.W. SUITE(A) UNISERVO VI-G MTU	PMO-403 UNIVAC 1544 MTU UNIVAC 610 CASSETTE	SPS-48 UNIVAC 1243 MTU UNIVAC 1231 PAPER TAPE	CLARINET MIRACLE KENNEDY 9000 MTU INTERCOMPUTER	ODS-DN UNIVAC 1243 MTU UNIVAC 1231 PAPER TAPE	ODS-SD UNIVAC 1540 MTU UNIVAC 1243 MTU	E.W. SUITE(B) INTELLIGENT MEM DISK	DASS REMEX 6375 PAPER TAPE KENNEDY 2330 CARTRIDGE	CMSGT CIPHER DATA PRO C-200 CASS. SINGER CL107MA-A DISK	ICAD UNIVAC 1240 MTU CIPHER C-2000 CASSETTE
CHAN 10	CHAN 10 CHAN 07	CHAN 10 CHAN 11	CHAN 16 CHAN 04	CHAN 14 CHAN 15	CHAN 11-15 CHAN 06	CHAN 14	CHAN 10 CHAN 14	CHAN 02 CHAN 01	CHAN 00 CHAN 04	CHAN 02-06 CHAN 01	CHAN 13-17 CHAN 13-17	CHAN 17	CHAN 01 CHAN 02	CHAN 00 CHAN 04	CHAN 04 CHAN 00
1-2	1 2	1 2	1 2	1 2	1 2	1-2	1 2	1 2	1 2	1 2	1 2	1-2	1 2	1 2	1 2
3-14	3-15	3-30	3-18	3-32	3-35	3-22	3-33	3-25	3-21	3-23	3-24	3-29	3-36	3-37	3-28

# AVAILABLE NDRO PROGRAM KIT CONFIGURATIONS (continued)

90536-7136335	HWLS UNIVAC 610 CASSETTE UNIVAC 1532 PAPER TAPE	CHAN 14 CHAN 04	1 2	3-38
90536-7136355	CDSSD(A) UNIVAC 1540 MTU UNIVAC 1243 MTU	CHAN 13-17 CHAN 13-17	1 2	3-49
90536-7136360	MAGIS(A) UNIVAC 1840M MTU INTERCOMPUTER	CHAN 10 CHAN 13	1 2	3-40
90536-7136376	ESMSP UNIVAC 1532 PAPER TAPE UNIVAC 1540 MTU	CHAN 14 CHAN 15	1 2	3-42
90536-7136385	MK-68 MK-68 GFCS PTR	CHAN 03	1-2	3-39
90536-7136390	MK-48(B) UNIVAC 1544 MTU CDO 844 DISK	CHAN 11-15 CHAN 13-17	1 2	3-41
90536-7136396	SOSUS-1 CAELUS 206-2 DISK KENNEDY 9000 MTU	CHAN 17 CHAN 11	1 2	3-16
90536-7136400	SSSMP(A) UNIVAC 1532 PAPER TAPE KENNEDY 9000 MTU	CHAN 01 CHAN 11	1 2	3-13
90536-7136405	NSRDC TRI DATA 120 CARTRIDGE KENNEDY 9000 MTU	CHAN 10 CHAN 14	1 2	3-9
90536-7136410	SANGUINE(A) PERTEC MTU 800 BPI REMX RR-0302 PAPER	CHAN 00 CHAN 01	1 2	3-10
90536-7136417	NAVMAOS UNIVAC 1532 PAPER TAPE UNIVAC CARTRIDGE MCTS	CHAN 15 CHAN 16	1 2	3-20
90536-7136420	LAMPS MOHAWK DATA SCI 2021 CART. UNIVAC 1540 MTU	CHAN 04 CHAN 12	1 2	3-31
90536-7136425	STMA UNIVAC 1870 CASSETTE KENNEDY 9000 MTU	CHAN 04 CHAN 14	1 2	3-44
90536-7136430	ISABPS TT/187 PAPER TAPE READER SYSTEM INDUSTRIES 3500 DISK	CHAN 07 CHAN 17	1 2	3-47
90536-7136435	SRD-18 UNIVAC 1870 CASSETTE	CHAN 04	1-2	3-46
90536-7136440	SANGUINE(B) AN/UGC-48A PAPER TAPE KENNEDY 2330 CARTRIDGE	CHAN 10 CHAN 05	1 2	3-43

# AVAILABLE NDRO PROGRAM KIT CONFIGURATIONS (continued)

90536-7136445	SANGUINE(C) KENNEDY 9000 MTU KENNEDY 2330 CARTRIDGE	CHAN 00 CHAN 05	1 2	3-26
90536-7136450	PAIR UNIVAC 1840M MTU UNIVAC 1532 PAPER TAPE	CHAN 00 CHAN 01	1 2	3-45
90536-7136455	WSC-2 NAVY ANTENNA CONTROL	CHAN --	1-2	3-53
90536-7136460	DDR UNIVAC DDR MTU READ/WRITE FILE	CHAN 00	1	3-50
90536-7136465	CMTU AN/USH-26 CMTU	CHAN 00	1	3-48
90536-7136475	SSES UNIVAC 1840M MTU TT-187 PAPER TAPE	CHAN 00 CHAN 07	1 2	3-34
90536-7136480	MK86 UNIVAC 1540 MTU UNIVAC 1532 PAPER TAPE	CHAN 00 CHAN 10	1 2	3-54
90536-7136490	CLASSIC CALIPER(B) DDC 7310 DISK AN/USH-26 CMTU	CHAN 04 CHAN 14	1 2	3-99
90536-7136500	SSES(B) KENNEDY 9000 MTU UNIVAC 1532 PAPER TAPE	CHAN 14 CHAN 04	1 2	3-17
90536-7136506	TRIDENT INTERCOMPUTER INTERCOMPUTER	CHAN 00 CHAN 01	1 2	3-51
90536-7136510	TRIDENT(B) INTERCOMPUTER OJ-172 DEAC MTU	CHAN 00 CHAN 02	1 2	3-63
90536-7136515	SEAFARER(A) AN/USH-26 CMTU KENNEDY 9000 MTU	CHAN 05 CHAN 00	1 2	3-56
90536-7136520	SEAFARER(B) AN/USH-26 CMTU UNIVAC 1532 PAPER TAPE	CHAN 05 CHAN 00	1 2	3-52
90536-7136527	ITAOC UNIVAC 1840M MTU PERTEC FLOPPY DISK	CHAN 03 CHAN 03	1 2	3-95
90536-7136531	ITBOIP UNIVAC 1232A PAPER TAPE UNIVAC 1540 MTU	CHAN 17 CHAN 12-16	1 2	3-72
90536-7136535	NTDS UNIVAC 1540 MTU UNIVAC 1231 PAPER TAPE	CHAN 03-07 CHAN 01	1 2	3-55

## AVAILABLE NDRO PROGRAM KIT CONFIGURATIONS (continued)

90536-7136540	ATLTYP4 CIPHER C-2000 CASSETTE KENNEDY 9000 MTU	CHAN 16 CHAN 00	1 2	3-60
90536-7136545	ATLTYP4(B) CIPHER DATA PRO C-200 CART. SINGER CL107MA-A DISK	CHAN 16 CHAN 17	1 2	3-68
90536-7136550	IRR UNISERVO VI-C MTU	CHAN 13	1-2	3-64
90536-7136555	IRR(B) SINGER CL107MA-A DISK POTTER MTU	CHAN 16 CHAN 14	1 2	3-75
90536-7136560	SOSUS-2 AN/USH-26 CMTU	CHAN 12	1	3-57
90536-7136566	SOSUS-3 AN/USH-26 CMTU INTERCOMPUTER	CHAN 00 CHAN 04	1 2	3-62
90536-7136570	SOSUS-4 AN/USH-26 CMTU SYSTEM INDUSTRIES 9500	CHAN 12 CHAN 11-15	1 2	3-61
90536-7136575	SURTASS UNIVAC 1870 CASSETTE SINGER LIBRASCOPE	CHAN 07 CHAN 17	1 2	3-81
90536-7136581	NTDS(B) UNIVAC 1243 MTU UNIVAC 1231 PAPER TAPE	CHAN 03-07 CHAN 01	1 2	3-69
90536-7136588	NAVMACS(B) AN/USH-26 CMTU RD-397 PAPER TAPE	CHAN 00 CHAN 01	1 2	3-59
90536-7136592	GYBFJP5 UNIVAC 1870 PAPER TAPE UNIVAC 1870 CASSETTE	CHAN 06 CHAN 06	1 2	3-77
90536-7136595	SQR-XX(B) AN/USH-26 CMTU KENNEDY 9000 MTU	CHAN 01 CHAN 14	1 2	3-58
90536-7136625	SQR-XX WANGCO DISK KENNEDY 9000 MTU	CHAN 17 CHAN 14	1 2	3-66
90536-7136631	SURTASS(B) UNIVAC 1870 CASSETTE SYSTEM INDUSTRIES 9500	CHAN 07 CHAN 11-15	1 2	3-74
90536-7136636	S58FC1G AN/USH-26 CMTU UNIVAC 1540 MTU	CHAN 17 CHAN 16	1 2	3-65
90536-7136640	JALBFP5 REMEX 6375 PAPER TAPE KENNEDY 9000 MTU	CHAN 00 CHAN 04	1 2	3-67

## AVAILABLE NDRO PROGRAM KIT CONFIGURATIONS (continued)

90536-7136650	SPS-48(B) OJ-172 DEAC PAPER TAPE OJ-172 DEAC MTU	CHAN 02-06 CHAN 02-06	1 2	3-70
90536-7136656	SPS-48(C) UNIVAC 1231 PAPER TAPE UNIVAC 1840M MTU	CHAN 01 CHAN 02-06	1 2	3-71
90536-7136663	PDS AN/USH-26 CMTU UNIVAC 1240 MTU	CHAN 03 CHAN 07	1 2	3-73
90536-7136667	MK23TAS AN/USH-26 CMTU KENNEDY 9000 MTU	CHAN 01 CHAN 00	1 2	3-78
90536-7136675	TSCT WANGCO DISK KENNEDY 9000 MTU	CHAN 17 CHAN 13	1 2	3-76
90536-7136685	AEGIS UNIVAC 1840M MTU INTERCOMPUTER	CHAN 10 CHAN 01-05	1 2	3-82
90536-7136690	TFCC UNIVAC 1840 MTU IBM RD-281 DISK	CHAN 01 CHAN 00	1 2	3-133
90536-7136825	SPS-48(D) UNIVAC 1243 MTU UNIVAC 1231 PAPER TAPE	CHAN 02-06 CHAN 01	1 2	3-85
90536-7136830	AEGIS(B) AN/USH-26 CMTU	CHAN 05	1	3-84
90536-7136835	LAMPS(A) OJ-172 DEAC MTU UNIVAC 1840M MTU	CHAN 02-06 CHAN 03-07	1 2	3-86
90536-7136841	JALBEA UNIVAC 1870 PAPER TAPE UNIVAC 1870 CASSETTE	CHAN 00 CHAN 00	1 2	3-83
90536-7136846	PLRS UNISERVO VI-C MTU AN/USH-26 CMTU	CHAN 00 CHAN 06	1 2	3-97
90536-7136851	SSMP(B) AN/USH-26 CMTU SINGER LIBRASCOPE	CHAN 01 CHAN 17	1 2	3-88
90536-7136855	ATLTYP4(C) WANGCO DISC KENNEDY 9000 MTU	CHAN 10 CHAN 00	1 2	3-87
90536-7136860	NCSL-CME CIPHER MTU DDC M6200-128 DISK	CHAN 00 CHAN 01	1 2	3-93
90536-7136865	IRR(C) UNIVAC 1540 MTU UNIVAC 1532 PAPER TAPE	CHAN 00 CHAN 16	1 2	3-90

## AVAILABLE NDRO PROGRAM KIT CONFIGURATIONS (continued)

90536-7136870	IRR(D) UNISERVO VI-C MTU SINGER CL107MA DISK	CHAN 13 CHAN 17	1 2	3-92
90536-7136876	ISABPS(B) TT/187 PAPER TAPE READER SYSTEM INDUSTRIES 3500 DISK	CHAN 01 CHAN 17	1 2	3-89
90536-7136880	MAGIS(C) UNIVAC 1840M MTU INTERCOMPUTER	CHAN 04 CHAN 07	1 2	3-105
90536-7136888	NAVMACS(C) AN/USH-26 CMTU RD-397 PAPER TAPE	CHAN 16 CHAN 15	1 2	3-91
90536-7136891	TACINTEL AN/USH-26 CMTU SYSTEM INDUSTRIES 3500 DISK	CHAN 00 CHAN 17	1 2	3-94
90536-7136896	OUTBOARD AN/USH-26 CMTU INTERCOMPUTER	CHAN 14 CHAN 02	1 2	3-96
90536-7136900	CCIS UNIVAC 1532 PAPER TAPE UNIVAC 610 CASSETTE	CHAN 00 CHAN 05	1 2	3-98
90536-7136915	SQR-19 AN/USH-26 CMTU IBM RASS DISK (AN/UYPH-7(V))	CHAN 01 CHAN 17	1 2	3-134
90536-7136920	AEGIS(C) AN/USH-26 CMTU UNIVAC 1840M MTU	CHAN 10 CHAN 14	1 2	3-120
90536-7136925	MK-68(B) UNIVAC 1840M MTU SPERRY GYRO PAPER TAPE	CHAN 00 CHAN 13	1 2	3-101
90536-7136930	SURTASS(C) KENNEDY 9000 MTU SYSTEM INDUSTRIES 9500 DISK	CHAN 07 CHAN 13-17	1 2	3-100
90536-7136935	AEGIS(D) UNIVAC 1840M MTU ODC 9762 DISK	CHAN 07 CHAN 13-17	1 2	3-104
90536-7136941	SPS-48(E) AN/USH-26 DRIVE 0 AN/USH-26 DRIVE 1	CHAN 01 CHAN 01	1 2	3-80
90536-7136946	COMDAC AN/USH-26 CMTU CL107MB SINGER DISK	CHAN 10 CHAN 11	1 2	3-102
90536-7136952	LAMPS(B) AN/USH-26 DRIVE 0 AN/USH-26 DRIVE 1 1540 MTU (SELECTED FROM M. PANEL)	CHAN 01 CHAN 01 CHAN 16	1 2 1-2	3-106

## AVAILABLE NDRO PROGRAM KIT CONFIGURATIONS (continued)

90536-7136955	POTS(B) UNIVAC 1243 MTU AN/USH-26 CMTU	CHAN 03-07 CHAN 01	1 2	3-103
90536-7136960	SEAFARER(C) KENNEDY 9000 MTU AN/USH-26 CMTU	CHAN 00 CHAN 11	1 2	3-108
90536-7136965	SEAFARER(D) AN/USH-26 CMTU CL107MA SINGER DISK	CHAN 04 CHAN 07	1 2	3-130
90536-7136970	RAPLOC UNIVAC 610 CASSETTE KENNEDY 9000 MTU	CHAN 00 CHAN 13	1 2	3-109
90536-7136975	ISPE AN/USH-26 CMTU SONAR DATA BUFFER	CHAN 17 CHAN 16	1 2	3-107
90536-7136980	RAPLOC(A) UNIVAC 1840M MTU INTERCOMPUTER	CHAN 03-07 CHAN 00-04	1 2	3-131
90536-7137025	TYQ AN/USH-26 CMTU PERTEC FLOPPY DISC	CHAN 03 CHAN 03	1 2	3-112
90536-7137035	AEGIS(E) AN/USH-26 CMTU UNIVAC 1840M MTU	CHAN 03 CHAN 07	1 2	3-119
90536-7137045	LINK-11 AN/USH-26 CMTU OJ-172 DEAC MTU	CHAN 01 CHAN 03-07	1 2	3-115
90536-7137055	NIPS UNIVAC 1840M MTU UNIVAC 1532 PAPER TAPE	CHAN 06 CHAN 12	1 2	3-121
90536-7137450	AEGIS(F) AN/USH-26 CMTU UNIVAC 1532 PAPER TAPE	CHAN 16 CHAN 00	1 2	3-110
90536-7137455	CANADA(B) AN/USH-26 CMTU REMEX 6375 PAPER TAPE	CHAN 10 CHAN 12	1 2	3-111
90536-7137598	TARTAR OJ-172 DEAC MTU OJ-172 DEAC PAPER TAPE	CHAN 17 CHAN 17	1 2	3-117
90536-7137603	SYS-1(B) AN/USH-26 CMTU UNIVAC 1545 DISK	CHAN 17 CHAN 07	1 2	3-126
90536-7137608	SYS-CG AN/USH-26 CMTU PDP-11/70 MTU	CHAN 01 CHAN 00	1 2	3-116

# AVAILABLE NDRO PROGRAM KIT CONFIGURATIONS (continued)

90536-7313613	CVNS UNIVAC 1540 MTU UNIVAC 1532 PAPER TAPE	CHAN 10 CHAN 00	1 2	3-114
90536-7313618	SYS-(1A) AN/USH-26 CMTU KENNEDY 9000 MTU	CHAN 17 CHAN 16	1 2	3-113
90536-7315663	VLS AN/USH-26 CMTU UNIVAC 1532 PAPER TAPE	CHAN 01 CHAN 04	1 2	3-118
90536-7315840	SEANYMPH GENISCO MD CLR-20 MTU DDC MDMS-20 6300 DISK	CHAN 13 CHAN 17	1 2	3-122
90536-7317896	NAVMACS(D) RD-433 DISK UNIT INTERCOMPUTER	CHAN 16 CHAN 14	1 2	3-124
90536-7317902	NAVMACS(E) AN/USH-26 CMTU INTERCOMPUTER	CHAN 16 CHAN 14	1 2	3-125
90536-7319748	SNSNTIF AN/USH-26 CMTU OJ-172 DEAC MTU	CHAN 01 CHAN 03-07	1 2	3-128
90536-7320706	CVNS(A) AN/USH-26 CMTU UNIVAC 1532 PTP RDR	CHAN 10 CHAN 15	1 2	3-129
90536-7321211	SURTASS(D) AN/UYH-3 DISK AN/USH-26 CMTU	CHAN 13 CHAN 14	1 2	3-127
90536-7321935	MAPS AN/USH-26 CMTU MICROPOLIS DISK	CHAN 00 CHAN 15	1 2	3-145
90536-7321986	OUTBOARD(A) EM* AN/UYH-7(V) DISK EM AN/UYH-7(V) DISK EM AN/USH-26 CMTU EM	CHAN 15 CHAN 07 CHAN 03	1 2	3-146
90536-7322652	CCSC AN/USH-26 CMTU UNIVAC 1545 DISK	CHAN 00 CHAN 17	1 2	3-151
90536-7322814	IRR (E) CL107MA DISK UNIT AN/USH-26 CMTU	CHAN 17,16 CHAN 14	1 2	3-152
90536-7323578	MK-68(C) UNIVAC 1840M MTU RAYMOND 6415 CART.	CHAN 00 CHAN 05	1 2	3-158

\* All bootstraps identified with an EM (Expanded Memory) were designed for the AN/UYK-20A computers. All bootstraps will run on either an expanded memory DPS or a DPS without expanded memory (within their limitations).

# AVAILABLE NDRO PROGRAM KIT CONFIGURATIONS (continued)

90536-7323584	NAVMACS(F) REV A RD-433 DISK UNIT INTERCOMPUTER	CHAN 16,17 CHAN 14,15	1 2	3-153
90536-7323874	NAVMACS (G) REV A INTERCOMPUTER AN/USH-26 CMTU	CHAN 14 CHAN 16	1 2	3-154
90536-7324696	TARTAR (A) EM* UNIVAC 1870 CASSETTE EM AN/USH-26 CMTU EM UNIVAC 1870 PTP RDR EM	CHAN 00 CHAN 02 CHAN 00	1 2 FROM M.P.	3-159
90536-7324757	IRR (F) CL107MA DISK UNIT AN/USH-26 CMTU	CHAN 17,16 CHAN 14	1 2	3-160
90356-7327092	B20F15 AN/USH-26 CMTU RD-358 (U1840M) MTU	CHAN 03 CHAN 13-17	1 2	3-165
90536-7327704	NAVMACS (H) AN/USH-26 CMTU RD-358 (U1840M) MTU	CHAN 01 CHAN 12-16	1 2	3-167
90536-7330301	RANDDG AN/USH-26 CMTU OJ-172 DEAC MTU	CHAN 01 CHAN 16	1 2	3-166
90536-7330302	SQR19AA AN/USH-26 CMTU INTERCOMPUTER	CHAN 01 CHAN 4,5	1 2	3-123
90536-7330303	NRIA UNIVAC 1543 MTU DDC MDMS-20 6300 DISK	CHAN 02 CHAN 17	1 2	3-132
90536-7332166	PATAFBT UNIVAC 1545 MTU UNIVAC 1543 MTU	CHAN 11 CHAN 13	1 2	3-169

\* All bootstraps identified with an EM (Expanded Memory) were designed for the AN/UYK-20A computers. All bootstraps will run on either an expanded memory DPS or a DPS without expanded memory (within their limitations).

# COMMON SERIAL I/O OPERATING MODE SELECTION INSTRUCTIONS

DESCRIPTION - Common serial I/O consists of two new serial interface kits which supersede all existing MIL-188C and RS-232C Interface Kits (refer to the following table).

COMMON SERIAL I/O KITS

DESCRIPTION	MIL-188C	RS-232C
KIT PART NUMBER	90536-7313567-02	90536-7313568-02
NOMENCLATURE	MK-2051/UYK-20(V)	MK-2048/UYK-20(V)
CARD TYPE I OR IA	90536-7312528-00	90536-7312528-00
CARD TYPE II OR III	90536-7312530-02	90536-7312670-04

The new cards use field alterable contact jumpers to permit interchangeability at the circuit card level. Use a needle-nose pliers to install and remove contact jumpers (90536-7098775-01).

INTERCHANGEABILITY AT THE CARD LEVEL - The common serial I/O Kit Type I/A card replaces all previous Type I/A cards and the Type II/III cards replace all previous Type II/III cards. Use the following procedure to replace an existing card.

1. Remove existing card, locate the card part number in Table Type I or IA or Table Type II or III, and determine appropriate jumper locations.
2. Install contact jumpers in TB1(J3) for Type I/A cards to match the configuration shown in Table Type I or IA. For Type II/III cards install contact jumpers in TB1(J3) and TB2(J4) as shown in Table Type II or III. The Configuration Definition Table defines symbols used in Table Type I or IA and Table Type II or III. See page 40 for TB locations.
3. Place new common serial card in the card jack occupied by the old card.

GROUP INSTALLATION - Group installation provides additional jumper selectable options. To select any mode place a jumper over the symbol representing that mode (see Table Type I or IA and Table Type II or III). Selection of sync/async can be incorporated at the channel level. For example, to make the odd channel sync mode, place a contact jumper over (SO) on Type I or IA and over (SO) on Type II or III. To make even channel async mode, place contact jumper over (AE) on Type I or IA and over (AE) on Type II or III. Two new asynchronous baud rates, 4800 and 9600, have been added. Also, an option has been added to allow the forced use of a single jumpered asynchronous baud rate independent of programmed selection, i.e., if only 9600 baud rate is selected, the two channel group will operate at 9600 baud rate regardless of programmed selection. Four baud rates may be selected for maximum use. A zero/one fill option is provided for input characters less than 8 bits in length. When running diagnostics, the zero/one fill option must be in the one's fill mode.

CONFIGURATION DEFINITION

TYPE I OR IA		
SYMBOL	MODE	J3(TB1)
SO	ODD CHANNEL SYNC	PINS 14 AND 15
AO	ODD CHANNEL ASYNC	PINS 13 AND 14
SE	EVEN CHANNEL SYNC	PINS 11 AND 12
AE	EVEN CHANNEL ASYNC	PINS 10 AND 11
RS	RS232C INTERFACE	PINS 8 AND 9
ML	MIL-188C INTERFACE	PINS 7 AND 8
1F	ONE'S FILL	PINS 5 AND 6
0F	ZERO FILL	PINS 4 AND 5
SP	SPARE JUMPER	PINS 1 AND 2

TYPE II OR III					
SYMBOL	MODE	J3(TB1)	SYMBOL	MODE	J4(TB2)
AE	EVEN CHANNEL ASYNC	PINS 11 AND 12	.75	75 BPS	PINS 15 AND 16
SE	EVEN CHANNEL SYNC	PINS 10 AND 11	1.5	150 BPS	PINS 13 AND 14
AO	ODD CHANNEL ASYNC	PINS 8 AND 9	3	300 BPS	PINS 11 AND 12
SO	ODD CHANNEL SYNC	PINS 7 AND 8	6	600 BPS	PINS 9 AND 10
SP	SPARE JUMPER	PINS 1 THROUGH 6	12	1200 BPS	PINS 7 AND 8
			24	2400 BPS	PINS 5 AND 6
			48	4800 BPS	PINS 3 AND 4
			96	9600 BPS	PINS 1 AND 2

TYPE I OR IA JUMPER LOCATIONS

90536 PART NUMBER	TB1 182 SP	TB1 743 SO	TB1 545 OF	TB1 545 1F	TB1 849 RS	TB1 10411 AE	TB1 11412 SE	TB1 13414 AO	TB1 14415 SO	CONNECTOR PINS SYMBOL
MIL-188C SYNC				X			X		X	
MIL-188C ASYNC				X				X		
RS232C SYNC					X				X	
RS232C ASYNC						X				

TYPE II OR III JUMPER LOCATIONS

90536 PART NUMBER	TB1 182 SP	TB1 743 SO	TB1 545 OF	TB1 545 1F	TB1 849 RS	TB1 10411 AE	TB1 11412 SE	TB1 13414 AO	TB1 14415 SO	TB2 182 SP	TB2 743 SO	TB2 545 1F	TB2 545 1F	TB2 849 RS	TB2 10411 AE	TB2 11412 SE	TB2 13414 AO	TB2 14415 SO	CONNECTOR PINS SYMBOL
MIL-188C SYNC				X															
MIL-188C ASYNC				X															
MIL-188C SYNC				X															
MIL-188C ASYNC				X															
MIL-188C SYNC				X															
MIL-188C ASYNC				X															
MIL-188C SYNC				X															
MIL-188C ASYNC				X															
MIL-188C SYNC				X															
MIL-188C ASYNC				X															
MIL-188C SYNC				X															
MIL-188C ASYNC				X															
MIL-188C SYNC				X															
MIL-188C ASYNC				X															
MIL-188C SYNC				X															
MIL-188C ASYNC				X															

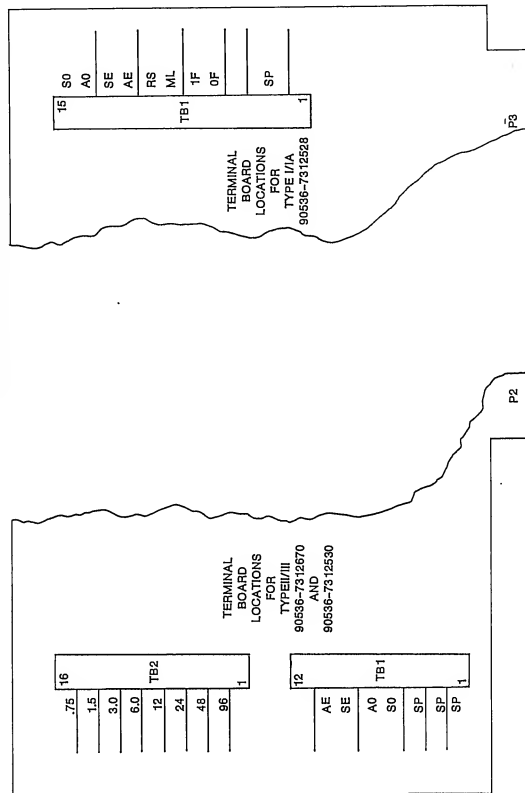
N/A IMPLIES NOT AVAILABLE

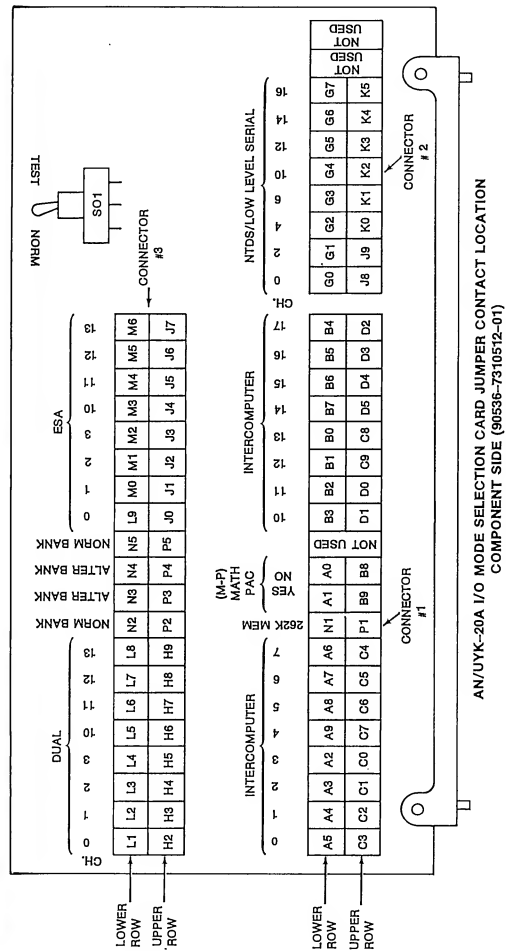
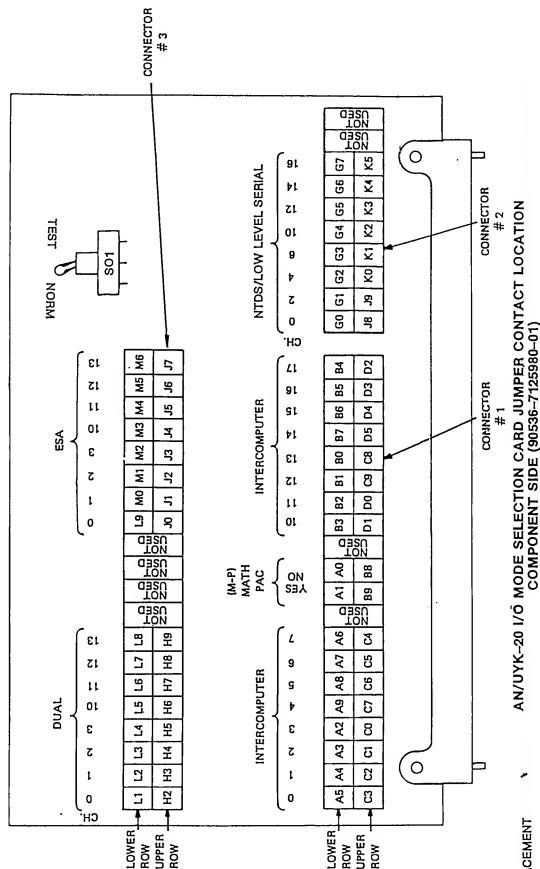
# TYPE II OR III JUMPER LOCATIONS (continued)

	90536 PART NUMBER	NATIONAL STOCK NUMBER	TB1 1-6 SP	TB1 788 SO	TB1 883 AO	TB1 10811 SE	TB2 182 AE	TB2 384 48	TB2 566 24	TB2 788 12	TB2 9810 6	TB2 11512 3	TB2 13514 1.5	TB2 15316 .75
MIL-188C ASYNC	7133291	7010 00 525 1383	SP		X		X	N/A	N/A	X	X			X
MIL-188C ASYNC	7133295	7010 00 525 1386	SP		X		X	N/A	N/A	X	X			
MIL-188C ASYNC	7133300	7010 00 525 1388	SP		X		X	N/A	N/A	X	X			
RS232C ASYNC	7133310	7010 00 575 2336	SP		X		X	N/A	N/A		X	X	X	X
RS232C ASYNC	7133315	5999 01 065 8309	SP		X		X	N/A	N/A		X	X	X	X
RS232C ASYNC	7133320	7010 LL HHA 1609			X		X	N/A	N/A	X		X	X	X
RS232C ASYNC	7133325	7010 LL HHA 1610			X		X	N/A	N/A	X	X	X	X	X
RS232C ASYNC	7133330	7010 01 003 6382	SP		X		X	N/A	N/A	X	X	X	X	X
RS232C ASYNC	7133335	7010 01 003 6386	SP		X		X	N/A	N/A	X	X		X	X
RS232C ASYNC	7133340	7010 LL HHA 1613	SP		X		X	N/A	N/A	X	X	X	X	X
RS232C ASYNC	7133345	7010 LL HHA 1614	SP		X		X	N/A	N/A	X	X	X	X	X
RS232C ASYNC	7133350	7010 01 003 6383	SP		X		X	N/A	N/A	X	X	X	X	X
RS232C ASYNC	7133355	5999 01 065 8310	SP		X		X	N/A	N/A	X	X	X	X	
RS232C ASYNC	7133360	7010 LL HHA 1617	SP		X		X	N/A	N/A	X	X	X	X	
RS232C ASYNC	7133365	7010 01 003 6380	SP		X		X	N/A	N/A	X	X	X	X	
RS232C ASYNC	7133370	7010 00 525 1414	SP		X		X	N/A	N/A	X	X	X	X	X
RS232C ASYNC	7132100	7010 01 003 6387	SP		X		X	N/A	N/A	X	X	X	X	
RS232C ASYNC	7132105	7010 00 575 2336	SP		X		X	N/A	N/A	X	X	X	X	
MIL-188C SYNC	7119441	7010 00 522 3590	SP	X		X		N/A	N/A					
RS232C SYNC	7119450	7010 00 575 2300	SP	X		X		N/A	N/A					

N/A IMPLIES NOT AVAILABLE

## TERMINAL BOARD LOCATIONS COMMON SERIAL PC ASSEMBLIES





SEE PAGES 45 AND 46 FOR JUMPER PLACEMENT

NOTE: PINS P1 AND N1 OF CONNECTOR NUMBER 1 MUST ALWAYS BE JUMPED IN THE AN/UYK-20A(V).



# I/O MODE SELECTION CARD JUMPER LOCATIONS\*

CHAN.	CONNECTOR 3 NORM (16-BIT)	CONNECTOR 3 DUAL (32-BIT)	CONNECTOR 3 ESA** (32-BIT)	CONNECTOR 1 IC*** (16,32)	CONNECTOR 2 NTDS/LOW LEVEL SERIAL (32-BIT)	CONNECTOR 3 VACALLES, 188C, OR 232C
0	Jumper L1 to H2	Remove L1 to H2	Jumper L9 to J0	Jumper A5 to C3	Jumper G0 to J8	Jumper L1 to H2
1	Jumper L2 to H3	Remove L2 to H3	Jumper M0 to J1	Jumper A4 to C2	-	Jumper L2 to H3
2	Jumper L3 to H4	Remove L3 to H4	Jumper M1 to J2	Jumper A3 to C1	Jumper G1 to J9	Jumper L3 to H4
3	Jumper L4 to H5	Remove L4 to H5	Jumper M2 to J3	Jumper A2 to C0	-	Jumper L4 to H5
4	See 0	See 0	See 0	Jumper A9 to C7	Jumper G2 to K0	See 0
5	See 1	See 1	See 1	Jumper A8 to C6	-	See 1
6	See 2	See 2	See 2	Jumper A7 to C5	Jumper G3 to K1	See 2
7	See 3	See 3	See 3	Jumper A6 to C4	-	See 3
10s	Jumper L5 to H6	Remove L5 to H6	Jumper M3 to J4	Jumper B8 to D1	Jumper G4 to K2	Jumper L5 to H6
11s	Jumper L6 to H7	Remove L6 to H7	Jumper M4 to J5	Jumper B2 to D0	-	Jumper L6 to H7
12s	Jumper L7 to H8	Remove L7 to H8	Jumper M5 to J6	Jumper B1 to C9	Jumper G5 to K3	Jumper L7 to H8
13s	Jumper L8 to H9	Remove L8 to H9	Jumper M6 to J7	Jumper B0 to C8	-	Jumper L8 to H9
14s	See 10s	See 10s	See 10s	Jumper B7 to D5	Jumper G6 to K4	See 10s
15s	See 11s	See 11s	See 11s	Jumper B6 to D4	-	See 11s
16s	See 12s	See 12s	See 12s	Jumper B5 to D3	Jumper G7 to K5	See 12s
17s	See 13s	See 13s	See 13s	Jumper B4 to D2	-	See 13s

\*Volume 3, Part 1, Figures 9-152 and 9-153.

Jumper in the selected position must be removed.

\*\*If IC channel is also to be dual or ESA, IC jumper only the lower channel of the pair.

NOTE: PINS P1 AND N1 OF CONNECTOR NUMBER 1 MUST ALWAYS BE JUMPED IN THE AN/UYK-20A(V).

# I/O MODE SELECTION CARD JUMPER REQUIREMENTS FOR AN/UYK-20 AND AN/UYK-20A

MODE SELECTED	CONNECTOR NUMBER	MODE SELECTION REQUIREMENTS										262K MEM	NORM BANK/ ALTER BANK
		IC JUMPER	NTDS/LOW SERIAL JUMPER	DUAL JUMPER	ES JUMPER	MATH PAC		TEST MODE SWITCH					
NORMAL	3	NO JUMPER	NO JUMPER	JUMPER	NO JUMPER	YES	NO	NO	NO	NORM	TEST	NOTE 5	
IC	1	JUMPER	NA	(1)	(1)	NA*	NA*	NA*	NA*	X	X		
NTDS/LOW LEVEL	2	NA	JUMPER	JUMPER	NO JUMPER	NA*	NA*	NA*	NA*	X	X		
SERIAL	3	(1)	NO JUMPER	NO JUMPER	NO JUMPER	NA*	NA*	NA*	NA*	X	X		
DUAL**	3	(1)	NO JUMPER	NO JUMPER	JUMPER	NA*	NA*	NO JUMPER	NA	X	NA		
ESA	3	(1)	NO JUMPER	NA	NA	JUMPER	AT- B9	AG-B8	NO JUMPER	NA	NA		
MATH PAC	1	NA	NA	NA	NA	AT- B9	AT- B9	NO JUMPER	NA	NA	NA		
NO MATH PAC	1	NA	NA	NA	NA	AT- B9	AT- B9	NO JUMPER	NA	NA	NA		
188C or VACALLES	3	NO JUMPER	NO JUMPER	JUMPER	NO JUMPER	NA*	NA*	NA*	NA*	X	X		
232C	3	NO JUMPER	NO JUMPER	JUMPER	NO JUMPER	NA*	NA*	NA*	NA*	X	X		
TEST MODE	SWITCH	(2)	(2)	(2)	(2)	NA*	NA*	NA*	NA*	(2)	(2)	NOTE 4 NOTE 3	NOTE 4 NOTE 3
EXPANDED	1	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		
MEMORY OPTION	3	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA		

X Denotes Select.

NA Denotes Not Applicable.

\* If Math Pac Option is available, connector 1 contacts A1-B9 must be jumpered. If Math Pac Option is not available, connector 1 contacts A0-B8 must be jumpered.

\*\* All unused dual channels must have jumpers installed, connector 3.

(1) If IC mode is desired with dual or ESA, on IC select only the lower numbered channel.

(2) If test position is selected, all channels will be forced into IC mode except the upper half of dual/ESA channels.

(3) NORM BANK - for normal numbering of memory banks (stacks 0,1,2,3 - BANK 0; stacks 4,5,6,7 - BANK 1) Jumper contacts N2 to P2 and N5 to P5.

ALTER BANK - for INTERLEAVING numbering of memory banks (stacks 0,2,4,6 - BANK 0; stacks 1,3,5,7 - BANK 1) Jumper contacts N3 to P3 and N4 to P4. (ALTER is to be used only with expanded memory)

(4) If DPS is an AN/UYK-20A, contact N1 must always be jumpered to P1.

(5) Expanded memory does not affect the jumpering of the other options, they remain the same as for the DPS with standard memory.

# AN/UYK-20 RETROFIT DEFINITION

The AN/UYK-20 is currently being retrofitted to correct anomalies inherent to hardware design. Retrofit I and II are complete. To identify the current retrofit status of an AN/UYK-20 the Field Change (FC) plate will be stamped with MPL or FCO numbers. It should be noted, however, that all AN/UYK-20 computers delivered after the last serial number of the respective MPLs will have been retrofitted in the factory and will not be stamped with the MPL or FCO number.

Example: AA817 will not be stamped with MPL-1534, MPL-1592 or MPL-1698.

The retrofit number, MPL or FCO number, and serial number affected by the MPL are identified in the table below:

RET. I MPL-1534

Serials A1-A325, A327, A328, A330-A342, A344-A347, A413, A436, A490

RET. II MPL-1592

Serials A1-A442, A444-A461, A463-488, A490-A504, A507, A512-A515, A517, A519, A520, A525-A527, A530, A533, A535, A544-A546, A552, A556, A567, A574, A581, A586, A635.

RET. III MPL-1698

Serials A1-A816

RET. IV FCO-151513

Serials A1-A794 with DMA, A1-AA1204 with NTDS Serial I/O, A1-AA1619 with 3 Phase - 60 Hz. Pwr. Sup., A160, A770, A795-AA1084, AA1092, AA1095, AA1099, AA1104, AA1110, AA1111, AA1115, AA1120, AA1166, AA1204.

RET. V

FCO 190706 Serials A1-AA1500 with PIC I/O  
FCO 190707 Serials AA1501-AA1672 with PIC I/O  
FCO 205294 Serials A1-B2609 with NTDS Serial I/O

All correspondence on retrofit status should be directed to NESEA Retrofit Coordinator:

Commanding Officer  
Naval Electronic Systems Engineering Activity  
St. Inigoes, MD 20684-0010  
Attn: Code 2251  
AN/UYK-20 ISEA  
AV: 356-3511/3512  
COM: 301-862-8815

## AN/UYK-20 PUBLICATIONS, EQUIPMENT, AND PROGRAM TAPES REQUIRED

QTY PER EQUIP.	NAME	DESIGNATION	REQUIRED USE
1	TECHNICAL MANUAL VOL. 1	SE610-AV-MMO-010 (NSN 0910-LP-043-7680)	TECHNICAL DOCUMENTATION
1	TECHNICAL MANUAL VOL. 2	SE610-AV-MMO-020 (NSN 0910-LP-043-7690)	REFERENCE DATA
1	TECHNICAL MANUAL VOL. 3 PART 1 VOL. 3 PART 2	SE610-AV-MMO-030 (NSN 0910-LP-043-7700)	EQUIPMENT DIAGRAMS
1	TECHNICAL MANUAL VOL. 4	SE610-AV-MMO-040 (NSN 0910-LP-043-7800)	DIAGNOSTIC OP PROCEDURES
1	TECHNICAL MANUAL VOL. 5	SE610-AV-MMO-050 (NSN 0910-LP-043-7900)	DIAGNOSTIC LISTINGS
1	TECHNICAL MANUAL VOL. 6	SE610-AV-MMO-060 (NSN 0910-LP-043-8000)	DIAGNOSTIC LISTINGS
1	TECHNICAL MANUAL VOL. 7	SE610-AV-MMO-070 (NSN 0910-LP-043-8100)	CONFIDENCE TESTS
1	HARDWARE USER'S GUIDE	SE610-AV-MMO-080 (NSN 0910-LP-043-8200)	CONFIDENCE TESTS
1	CP/MEMORY DIAGNOSTIC PROGRAM TAPE	TE610-AD-SWP-010	TROUBLESHOOTING
1	I/O DIAGNOSTIC PROGRAM TAPE	TE610-AD-SWP-020	TROUBLESHOOTING
1	OPTIONS DIAGNOSTIC PROGRAM TAPE	TE610-AD-SWP-030	TROUBLESHOOTING
1	CONFIDENCE TEST (56K) PROGRAM TAPE(S)	TE610-AD-SWP-040	CONFIDENCE TESTING
1	CONFIDENCE (24K), CP/MEMORY PROGRAM TAPE	TE610-AD-SWP-050	CONFIDENCE TESTING
1	CONFIDENCE TEST (24K), I/O PROGRAM TAPE	TE610-AD-SWP-060	CONFIDENCE TESTING
1	CONFIDENCE TEST (24K), OPTIONS PROGRAM TAPE	TE610-AD-SWP-070	CONFIDENCE TESTING
*	MICRO GROWTH 1 DIAGNOSTIC TAPE	TE610-AD-SWP-080	TROUBLESHOOTING MICRO GROWTH 1 CARD
*	MICRO GROWTH 2 DIAGNOSTIC TAPE	TE610-AD-SWP-090	TROUBLESHOOTING MICRO GROWTH 2 CARD
*	MICRO GROWTH 3 DIAGNOSTIC TAPE	TE610-AD-SWP-100	TROUBLESHOOTING MICRO GROWTH 3 CARD
*	MICRO GROWTH 4 DIAGNOSTIC TAPE	TE610-AD-SWP-110	TROUBLESHOOTING MICRO GROWTH 4 CARD
1	SINGLE CHANNEL JUMPER PLUG, PARALLEL	90536-7150225-00 (NSN 5935-01-089-5457) OR -7126394-00 (NSN 7010-01-019-1541)	I/O END-AROUND JUMPERING (CHANNELS 0-3)
2	SINGLE CHANNEL JUMPER PLUG, PARALLEL	90536-7150226-00 (NSN 5935-01-089-5458) OR -7126394-00 (NSN 7010-01-019-1541)	I/O END-AROUND JUMPERING (CHANNELS 4-17)

\*ITEMS ARE REQUIRED ONLY IF THOSE OPTIONS ARE CONFIGURED INTO THE DPS.

AN/UYK - 20 PUBLICATIONS, EQUIPMENT, AND PROGRAM TAPES REQUIRED  
(continued)

QTY PER EQUIP	NAME	DESIGNATION	REQUIRED USE
1	SINGLE CHANNEL JUMPER PLUG, SERIAL	90536-7150233-00 (NSN 5935-01-089-5459)	I/O JUMPERING OF SERIAL CHANNELS (1888C, RS232C, VACALES)
*	CROSS CHANNEL WRAP-AROUND CABLE, SERIAL	90536-7103939-00	I/O JUMPING OF SERIAL CHANNELS (188C, RS232C, VACALES)
*	EXTERNAL FUNCTION GENERATOR	VARIABLE	PROVIDE EXTERNAL CLOCK FOR SYNC CHANNELS
*	32-BIT (DUAL) CHANNEL JUMPER PLUG, PARALLEL	90536-7126375-00 (INPUT) (NSN 7010-01-100-3217) 90536-7126375-01 (OUTPUT) (NSN 7010-01-100-3218) 90535-7903056-03 (NSN 5120-00-126-7282) 90536-7100905-00 (NSN 7010-00-602-6004) 90536-7134954-00 (Right-Hand) (NSN 7010-01-003-6117) 90536-7134953-00 (Left-Hand) (NSN 7010-00-602-6003) NAVSEA RE-E5033644	TO PERMIT 32-BIT (DUAL PARALLEL CHANNEL OPERATION) OPEN CABINET
1	HEX-HEAD DRIVER	90535-7903056-03 (NSN 5120-00-126-7282) 90536-7100905-00 (NSN 7010-00-602-6004)	REMOVE CP LOGIC PC CARDS
1	LOGIC CARD EXTRACTOR	90536-7134954-00 (Right-Hand) (NSN 7010-01-003-6117)	REMOVE I/O AND MEMORY PC CARDS
1	MEMORY CARD EXTRACTOR	90536-7134953-00 (Left-Hand) (NSN 7010-00-602-6003) NAVSEA RE-E5033644	
REF DATA	OUTLINE AND INSTALLATION DWG DRAWING LIST BLOCK DIAGRAM CABLE RUN DIAGRAM SUMMARY OF INSTALL MLT I/O SHEETS	NAVSEA RE-E5033644 NAVSEA RE-E5033996 NAVSEA RE-D5033642 NAVSEA RE-A5033640 NAVSEA RE-C5033641 NAVSEA RE-D5033643	

\* ITEMS ARE REQUIRED ONLY IF THOSE OPTIONS ARE CONFIGURED INTO THE DPS.  
THE PROGRAM TAPES LISTED ARE AVAILABLE FROM:

COMMANDING OFFICER  
NAVAL ELECTRONIC SYSTEM ENGINEERING ACTIVITY  
ST. INGOES, MD 20684 - 0010  
ATTN: CODE 2251  
AN/UYK - 20 ISEA  
AV: 356 - 3511/3512

AN/UYK - 20 PUBLICATIONS, EQUIPMENT, AND PROGRAM TAPES REQUIRED

QTY PER EQUIP	NAME	DESIGNATION	REQUIRED USE
1	TECHNICAL MANUAL VOL. 1	SE510-A3-MMO-010 (NSN 0910-LP-302-8500)	TECHNICAL DOCUMENTATION REFERENCE DATA
1	TECHNICAL MANUAL VOL. 2	SE510-A3-MMO-020 (NSN 0910-LP-302-8500)	
1	TECHNICAL MANUAL VOL. 3	SE510-A3-MMO-030 (NSN 0910-LP-302-8700)	EQUIPMENT DIAGRAMS
1	TECHNICAL MANUAL VOL. 4	SE510-A3-MMO-040 (NSN 0910-LP-302-8800)	DIAGNOSTIC OP PROCEDURES
1	TECHNICAL MANUAL VOL. 5	SE510-A3-MMO-050 (NSN 0910-LP-302-8900)	DIAGNOSTIC LISTINGS
1	TECHNICAL MANUAL VOL. 6	SE510-A3-MMO-060 (NSN 0910-LP-302-9000)	DIAGNOSTIC LISTINGS
1	TECHNICAL MANUAL VOL. 7	SE510-A3-MMO-070 (NSN 0910-LP-302-9100)	CONFIDENCE TESTS
1	HARDWARE USER'S GUIDE	SE510-A3-GYD-010	
1	CP/MEMORY DIAGNOSTIC PROGRAM TAPE	TE610-AL-SWP-01A	TROUBLESHOOTING
1	I/O DIAGNOSTIC PROGRAM TAPE	TE610-AL-SWP-02A	TROUBLESHOOTING
1	OPTIONS DIAGNOSTIC PROGRAM TAPE	TE610-AL-SWP-03A	TROUBLESHOOTING
1	CONFIDENCE TEST (56K) PROGRAM TAPE(S)	TE610-AL-SWP-04A	CONFIDENCE TESTING
1	CONFIDENCE (24K), CP/MEMORY PROGRAM TAPE	TE610-AL-SWP-05A	CONFIDENCE TESTING
1	CONFIDENCE TEST (24K), I/O PROGRAM TAPE	TE610-AL-SWP-06A	CONFIDENCE TESTING
1	CONFIDENCE TEST (24K), OPTIONS PROGRAM TAPE	TE610-AL-SWP-07A	CONFIDENCE TESTING
*	MICRO GROWTH 1 DIAGNOSTIC TAPE	TE510-AL-SWP-080	TROUBLESHOOTING MICRO GROWTH 1 CARD
*	MICRO GROWTH 2 DIAGNOSTIC TAPE	TE610-AL-SWP-090	TROUBLESHOOTING MICRO GROWTH 2 CARD
*	MICRO GROWTH 3 DIAGNOSTIC TAPE	TE610-AL-SWP-100	TROUBLESHOOTING MICRO GROWTH 3 CARD
*	MICRO GROWTH 4 DIAGNOSTIC TAPE	TE610-AL-SWP-11A	TROUBLESHOOTING MICRO GROWTH 4 CARD
1	SINGLE CHANNEL JUMPER PLUG, PARALLEL	90536-7150225-00 (NSN 5935-01-089-5457) OR -7126394-00 (NSN 7010-01-019-1541)	I/O END-AROUND JUMPERING (CHANNELS 0-3)
2	SINGLE CHANNEL JUMPER PLUG, PARALLEL	90536-7150226-00 (NSN 5935-01-089-5458) OR -7126394-00 (NSN 7010-01-019-1541)	I/O END-AROUND JUMPERING (CHANNELS 4-17)
1	SINGLE CHANNEL JUMPER PLUG, SERIAL	90536-7150233-00 (NSN 5935-01-089-5459)	I/O JUMPERING OF SERIAL CHANNELS (1888C, RS232C, VACALES)

\*ITEMS ARE REQUIRED ONLY IF THOSE OPTIONS ARE CONFIGURED INTO THE DPS.

AN/UYK - 20 PUBLICATIONS, EQUIPMENT, AND PROGRAM TAPES REQUIRED  
(continued)

QTY PER EQUIP.	NAME	DESIGNATION	REQUIRED USE
*	CROSS CHANNEL WRAP-AROUND CABLE SERIAL	90536-7103939-00	I/O JUMPING OF SERIAL CHANNELS (188C, RS232C, VACALCS)
*	EXTERNAL FUNCTION GENERATOR	VARIABLE	PROVIDE EXTERNAL CLOCK FOR SYNC CHANNELS
*	32-BIT (DUAL) CHANNEL JUMPER PLUG, PARALLEL	90636-7126375-00 (INPUT) (NSN 7010-01-100-3217) 90536-712675-01 (OUTPUT) (NSN 7010-01-100-3219)	TO PERMIT 32-BIT (DUAL PARALLEL CHANNEL OPERATION)
1	HEX-HEAD DRIVER	90536-7303056-03 (NSN 5120-00-126-7282)	OPEN CABINET
1	LOGIC CARD EXTRACTOR	90536-7100903-00 (NSN 7010-00-602-6004)	REMOVE CP LOGIC PC CARDS
1	MEMORY CARD EXTRACTOR	90536-7149954-00 (Right-Hand) (NSN 7010-01-003-6117) 90536-7134953-00 (Left-Hand) (NSN 7010-00-602-6003)	REMOVE I/O AND MEMORY PC CARDS
REF DATA	OUTLINE AND INSTALLATION DWG DRAWING LIST BLOCK DIAGRAM CABLE RUN SHEETS SUMMARY OF INSTALL MLTS I/O SHEETS	NAVSEA RE-B5033696 NAVSEA RE-D5033642 NAVSEA RE-A5033640 NAVSEA RE-D5033641 NAVSEA RE-D5033643	

\*ITEMS ARE REQUIRED ONLY IF THOSE OPTIONS ARE CONFIGURED INTO THE DPS.  
THE PROGRAM TAPES LISTED ARE AVAILABLE FROM:

COMMANDING OFFICER  
NAVAL ELECTRONIC SYSTEMS ENGINEERING ACTIVITY  
ST. INIGOES, MD 20684-0010  
ATTN: CODE 2251  
AV: NA/UYK-00 ISEA  
356-3511/8512  
COM: 301-862-6815

AN/UYK-20 REPLACEMENT ASSEMBLIES LIST

PART NUMBER	SUPERSEDES	SUPERSEDED BY	PART NUMBER	SUPERSEDES	SUPERSEDED BY
905411-04	-	7150314-00	7125156-01	7125155-01	7125157-01
905411-06	-	7150314-01	7125157-01	7125156-01	-
7092030-01	-	7092031-01	7125175-01	-	-
7092031-01	7092030-01	7092030-01	7125235-01	7125236-01	7125239-01
7092032-01	7092031-01	7125236-01	7125236-01	7125235-01	7125237-01
7092175-01	-	7092176-01	7125237-01	7125236-01	-
7092176-01	7092175-01	7150210-01	7125240-01	-	7125241-01
7092181-01	-	7136265-01	7125241-01	7125240-01	-
7092185-01	-	7092187-01	7125275-01	-	7125276-01
7092187-01	7092185-01	-	7125276-01	7125275-01	-
7092195-01	-	-	7125290-01	-	7125291-01
7092200-01	-	7092201-01	7125305-01	-	7125306-01
7092201-01	7092200-01	-	7125306-01	7125305-01	7125307-01
7101824-01	-	7101824-02	7125307-01	7125306-01	-
7101824-02	7101824-01	7101824-03	7125310-01	-	7125311-01
7101824-03	7101824-02	-	7125311-01	7125310-01	-
7101840-00	-	7135560-00	7125310-01	-	-
7101875-00	-	7135561-00	7125385-01	-	7125386-01
7101880-00	-	7150352-00	7125386-01	7125385-01	7125387-01
7101885-00	-	7135563-00	7125387-01	7125386-01	7150400-01
7101963-01	-	-	7125405-01	-	7125406-01
7101963-02	-	-	7125406-01	7125405-01	-
7101966-01	-	-	7125415-01	-	7125416-01
7101966-02	-	-	7125416-01	7125415-01	7125417-01
7101990-00	-	7135564-00	7125417-01	-	-
7101995-00	-	7135565-00	7125500-01	-	-
7118316-01	-	7150465-01	7125510-01	-	7150665-01
7119380-01	-	-	7125511-01	-	7125512-01
7119385-01	-	7132152-01	7125565-01	7125566-01	7150220-01
-	-	-02	7125566-01	-	7125567-01
-	-	-03	7125592-01	-	7125592-01
7119390-01	-	7132154-01	7125592-01	7125592-01	7125592-01
-	-	-02	7125960-01	7092032-01	7125961-01
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7119405-01	-	7132150-01	7126070-01	7126071-01	7137000-01
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7125150-01	-	7125151-01	7126382-04	-	7128082-00
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PART NUMBER	SUPERSEDES	SUPERSEDED BY	PART NUMBER	SUPERSEDES	SUPERSEDED BY	PART NUMBER	SUPERSEDES	SUPERSEDED BY	PART NUMBER	SUPERSEDES	SUPERSEDED BY
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		-02,		-	-01,	7133949-01	-	7306823-01	-	-	-
7132105-01	-	7312670-00,		-	-02	7134942-01	-	-	7136423-01	-	-
		-02,	7133270-01	7133270-01	7312530-00,	7134942-01	-	-	7136430-01	-	-
		-04	7133271-01	-	-01,	7134974-02	-	7308013-00	7136435-01	-	-
7132110-01	-	7312148-01		-	-02	7134974-03	7133934-02	7308013-01	7136440-01	-	-
7132115-01	-	7312121-01	7133275-01	-	7312530-00,	7134994-01	7134994-02	7134994-02	7136445-01	-	-
7132120-01	-	-02,		-	-01,	7134994-02	7134994-01	7134994-03	7136450-01	-	-
		-03		-	-02	7134994-03	7134994-02	-	7136460-01	-	-
7132121-01	7132120-01	-	7133280-01	-	7312530-00,	7134998-00	-	-	7136465-01	-	-
7132121-02	7132120-01	-		-	-01,	7134998-01	-	-	7136475-01	-	-
7132121-03	7132120-01	-	7133285-01	-	-02	7135560-00	7101840-00	7150350-00	7136480-01	-	-
7132125-01	-	7132126-01		-	-01,	7135561-00	7101875-00	7150351-00	7136490-01	-	-
7132126-01	7132125-01	-		-	-02	7135563-00	7101885-00	7150353-00	7136500-01	-	-
7132130-01	-	7312131-01,	7133290-01	7133290-01	7312530-00,	7135564-00	7101990-00	7150354-00	7136505-01	7136506-01	-
		-02,	7133291-01	-	-01,	7135565-00	7101995-00	7150355-00	7136510-01	-	-
		-03		-	-02	7135570-01	-	7135570-02	7136515-01	-	-
7132131-01	7132130-01	-		-	-03	7135570-01	7135570-01	7150383-01	7136520-01	-	-
7132131-02	7132130-01	-	7133295-01	-	7312530-00,	7135570-02	7135570-03	7150383-01	7136525-01	7136526-01	7136526-01
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7132146-01	7119401-01	7132146-11,		-	-02	7136170-01	-	-	7136535-01	-	-
		-12,	7133305-01	-	7133306-01	7136185-01	-	7136186-01	7136540-01	-	-
		-13	7133306-01	7133305-01	7312528-00	7136186-01	7136185-01	-	7136545-01	-	-
7132146-11	7132146-01	-	7133310-01	-	7312670-00,	7136190-01	-	-	7136550-01	-	-
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7132148-13	7132148-01	-		-	-04	7136230-01	-	-	7136585-01	-	-
7132150-01	7119405-01	-	7133325-01	-	7312670-00,	7136235-01	-	-	7136590-01	7136587-01	7136588-01
7132150-03	7119405-01	-		-	-02,	7136245-01	-	-	7136591-01	-	-
7132152-01	7119385-01	-		-	-04	7136250-01	-	-	7136595-01	-	-
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7132199-01	-	7132197-00		-	-02,	7136310-01	-	-	7136665-01	-	-
7132225-01	-	7132226-01		-	-04	7136315-01	-	-	7136670-01	-	-
7132226-01	7132225-01	7132227-01	7133355-01	-	7312670-00,	7136320-01	-	-	7136675-01	-	-
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7132235-01	-	7312530-00,		-	-04	7136350-01	7126181-01	7136351-01	7136705-01	7136700-01	-
		-01,	7133365-01	-	7312670-00,	7136355-01	7136350-01	-	7136710-01	-	-
		-02		-	-04	7136360-01	-	-	7136715-01	-	-
7133240-01	-	7312530-00,	7133370-01	-	7312670-00,	7136370-01	-	7136371-01	7136720-01	-	-
		-01,		-	-02,	7136375-01	7136370-01	-	7136725-01	-	-
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		-01,	7133934-00	7133934-00	-	7136420-01	-	-	7136770-01	-	-
		-02	7133934-01	7133934-01	-	7136425-01	-	-	7136775-01	-	-
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		-02		-	-04	7136440-01	-	-	7136790-01	-	-
		-03		-	-04	7136445-01	-	-	7136795-01	-	-
		-04		-	-04	7136450-01	-	-	7136800-01	-	-
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		-07		-	-04	7136465-01	-	-	7136815-01	-	-
		-08		-	-04	7136470-01	-	-	7136820-01	-	-
		-09		-	-04	7136475-01	-	-	7136825-01	-	-
		-10		-	-04	7136480-01	-	-	7136830-01	-	-
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		-12		-	-04	7136490-01	-	-	7136840-01	-	-
		-13		-	-04	7136495-01	-	-	7136845-01	-	-
		-14		-	-04	7136500-01	-	-	7136850-01	-	-
		-15		-	-04	7136505-01	-	-	7136855-01	-	-
		-16		-	-04	7136510-01	-	-	7136860-01	-	-
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		-18		-	-04	7136520-01	-	-	7136870-01	-	-
		-19		-	-04	7136525-01	-	-	7136875-01	-	-
		-20		-	-04	7136530-01	-	-	7136880-01	-	-
		-21		-	-04	7136535-01	-	-	7136885-01	-	-
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		-23		-	-04	7136545-01	-	-	7136895-01	-	-
		-24		-	-04	7136550-01	-	-	7136900-01	-	-
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		-29		-	-04	7136575-01	-	-	7136925-01	-	-
		-30		-	-04	7136580-01	-	-	7136930-01	-	-
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		-36		-	-04	7136610-01	-	-	7136960-01	-	-
		-37		-	-04	7136615-01	-	-	7136965-01	-	-
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		-39		-	-04						

PART NUMBER	SUPERSEDES	SUPERSEDED BY	PART NUMBER	SUPERSEDES	SUPERSEDED BY
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7136870-01	-	-	7150383-00	7135570-02	7150383-02
7136875-01	-	7136876-01	7150383-01	7135570-03	7150383-03
7136876-01	7136875-01	-	7150383-02	7150383-00	7308028-00
7136880-01	-	-	7150383-03	7150383-01	7309028-01
7136885-01	-	7136886-01	7150395-01	7126137-01	7150396-01
7136886-01	7136885-01	-	7150396-01	7150395-01	7150397-01
7136887-01	7136886-01	-	7150397-01	7150396-01	-
7136888-01	7136887-01	-	7150400-01	7125387-01	7150401-01
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7136895-01	-	7136896-01	7150415-01	-	-
7136896-01	7136895-01	-	7150420-01	7126186-01	7150421-01
7136900-01	-	-	7150421-01	7150420-01	-
7136905-01	7136371-01	-	7150460-01	-	7150465-01
7136915-01	-	-	7150465-01	7118316-01	-
7136920-01	-	-	7150465-01	7125510-01	-
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7136935-01	-	-	7150480-01	7126207-01	-
7136940-01	-	7136941-01	7150486-00	7126264-00	-
7136941-01	7136940-01	-	7150490-00	7126286-00	-
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7136951-01	7136950-01	-	7308013-01	7134974-03	-
7136952-01	7136951-01	-	7308028-00	7150383-02	-
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7136965-01	-	-	7309623-00	7133943-00	-
7136970-01	-	-	7309623-01	7133943-01	-
7136975-01	-	-	7310014-06	-	7310014-08
7136980-01	-	-	7310014-07	-	7310014-09
7137000-01	7126071-01	-	7310014-08	-	-
7137025-01	-	-	7310014-09	-	-
7137035-01	-	-	7310022-18	-	-
7137045-01	-	-	7310510-01	-	-
7137070-01	-	-	7310512-01	-	-
7137130-01	-	7137130-02	7310514-01	-	7310514-02
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7150295-01	7150322-01	-	7310522-01	-	-
7150304-00	-	-	7310524-01	-	-
7150314-00	905411-04	-	7310526-01	-	-
7150314-01	905411-06	-	7310534-01	-	7310534-02
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7150338-01	-	-	7310536-01	-	7310536-02
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7150350-02	7150350-01	-	7310690-01	7310326-01	7312344-01
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7150353-02	7150353-01	7150353-03	7312528-00	7119446-01	-
7150353-03	7150353-02	-	7312528-01	7119437-01	-
7150353-04	7150353-03	-	7312528-02	7139227-01	-
7150354-00	7150354-00	7150354-01	7312528-03	7150356-01	-
7150354-01	7150354-00	7150354-02	7312530-00	7119441-01	-
7150354-02	7150354-01	7150354-03	7312530-01	7313231-01	-
7150354-03	7150354-02	7150354-04	7312530-02	7133235-01	-
7150354-04	7150354-03	-	7312530-03	7133240-01	-
7150355-00	7135565-00	7150355-01	7312530-04	7133245-01	-

PART NUMBER	SUPERSEDES	SUPERSEDED BY	PART NUMBER	SUPERSEDES	SUPERSEDED BY
7312530-00	7133250-01	-	7312670-04	7133310-01	-
7312530-00	7133255-01	-	7312670-04	7133315-01	-
7312530-00	7133260-01	-	7312670-04	7133320-01	-
7312530-00	7133265-01	-	7312670-04	7133325-01	-
7312530-00	7133271-01	-	7312670-04	7133330-01	-
7312530-00	7133275-01	-	7312670-04	7133335-01	-
7312530-00	7133280-01	-	7312670-04	7133340-01	-
7312530-00	7133285-01	-	7312670-04	7133345-01	-
7312530-00	7133291-01	-	7312670-04	7133350-01	-
7312530-00	7133295-01	-	7312670-04	7133355-01	-
7312530-00	7133300-01	-	7312670-04	7133360-01	-
7312530-01	7119441-01	-	7312670-04	7133365-01	-
7312530-01	7133231-01	-	7312670-04	7133370-01	-
7312530-01	7133235-01	-	7312682-06	-	7312682-07
7312530-01	7133240-01	-	7312682-07	7312682-06	-
7312530-01	7133245-01	-	7313055-01	-	-
7312530-01	7133250-01	-	7313055-01	-	-
7312530-01	7133255-01	-	7313055-01	-	-
7312530-01	7133260-01	-	7313055-13	-	-
7312530-01	7133265-01	-	7313598-01	-	-
7312530-01	7133271-01	-	7313603-01	-	-
7312530-01	7133275-01	-	7313608-01	-	-
7312530-01	7133280-01	-	7313613-01	-	-
7312530-01	7133285-01	-	7313618-01	-	-
7312530-01	7133291-01	-	7314830-01	-	-
7312530-01	7133295-01	-	7315270-01	-	-
7312530-01	7133300-01	-	7315663-01	-	-
7312530-02	7119441-01	-	7315840-01	-	-
7312530-02	7133231-01	-	7316476-00	-	7316476-01
7312530-02	7133235-01	-	7316476-01	7316476-00	7316476-02
7312530-02	7133240-01	-	7316476-02	7316476-01	-
7312530-02	7133245-01	-	7316476-02	-	7316476-01
7312530-02	7133250-01	-	7316476-02	7316476-00	7316476-02
7312530-02	7133255-01	-	7316476-02	7316476-01	7316476-03
7312530-02	7133260-01	-	7316476-03	7316476-02	7316476-04
7312530-02	7133265-01	-	-	-	-05
7312530-02	7133271-01	-	-	-	-06
7312530-02	7133275-01	-	7316476-04	7316476-03	7316476-07
7312530-02	7133280-01	-	7316476-05	7316476-03	7316476-07
7312530-02	7133285-01	-	7316476-06	7316476-03	7316476-07
7312530-02	7133291-01	-	7316476-07	7316476-04	-
7312530-02	7133295-01	-	-	-05	-
7312530-02	7133300-01	-	-	-06	-
7312670-00	7119450-01	-	7316994-00	-	-
7312670-00	7312100-01	-	7316994-01	-	-
7312670-00	7312105-01	-	7317896-01	-	-
7312670-00	7313010-01	-	7317902-01	-	-
7312670-00	7313315-01	-	7317908-01	-	7321211-01
7312670-00	7313320-01	-	7319065-01	-	7330300-01
7312670-00	7313325-01	-	7317272-01	-	7330303-01
7312670-00	7313330-01	-	7317478-01	-	-
7312670-00	7313335-01	-	7320637-01	-	7321244-01
7312670-00	7313340-01	-	7320706-01	-	-
7312670-00	7313345-01	-	7321211-01	7317908-01	-
7312670-00	7313350-01	-	7321244-01	7320637-01	7321624-01
7312670-00	7313355-01	-	7321528-01	-	-
7312670-00	7313360-01	-	7321618-01	-	-
7312670-00	7313365-01	-	7321624-01	7321244-01	-
7312670-00	7313370-01	-	7321935-01	-	-
7312670-00	7119450-01	-	7321986-01	-	-
7312670-00	73132100-01	-	7322151-01	-	-
7312670-00	73132105-01	-	7322535-01	-	-
7312670-00	7313310-01	-	7322536-01	-	-
7312670-00	7313315-01	-	7322652-01	-	-
7312670-00	7313320-01	-	7322814-01	-	-
7312670-00	7313325-01	-	7323146-01	-	7323584-01
7312670-00	7313330-01	-	7323152-01	-	7323561-01
7312670-00	7313335-01	-	7323179-01	-	-
7312670-00	7313340-01	-	7323371-01	-	-
7312670-00	7313345-01	-	7323538-01	-	-
7312670-00	7313350-01	-	7323561-01	7323152-01	7323874-01
7312670-00	7313355-01	-	7323578-01	-	-
7312670-00	7313360-01	-	7323584-01	7323146-01	-
7312670-00	7313365-01	-	7323597-01	7323561-01	-
7312670-00	7313370-01	-	7324151-01	-	-
7312670-04	7119450-01	-	7324596-01	-	-
7312670-04	7312100-01	-	7324757-01	-	-
7312670-04	7312105-01	-	7327092-01	-	-

PART NUMBER	SUPERSEDES	SUPERSEDED BY
7327170-01	-	7330301-01
7327704-01	-	-
7330301-01	7327170-01	-
7330302-01	7319065-01	-
7330303-01	7319072-01	-
7332166-01	-	-

The procedures contained in the following paragraphs provide abbreviated instructions necessary to execute the Diagnostic Programs. Any errors detected while executing these procedures are explained in SE810-AV-MM0-050 paragraphs 11-16 through 11-27 for the AN/UYK-20, and in SE810-A3-MM0-040 paragraphs 11-16 through 11-27 for the AN/UYK-20A.

## Microdiagnostic Program Execution Procedure

1. Stop and Master Clear
2. Initial switch settings

ALTER MODE SET/CLR	SET
PROCESSOR DISABLE RT CLK	INT
PROCESSOR DISABLE ADV P	DOWN
PROCESSOR DISABLE INTER CMPTR TIME OUT	DOWN
BREAK PT READ/OFF	OFF
BREAK PT WRITE/OFF	OFF

3. Press DISPLAY SELECT CLR. DISPLAY NUMBER = 0
4. Press MODE MICRO STEP
5. Set DIAGNOSTIC DISPLAY switch down and DIAGNOSTIC JUMP switch to up
6. Press MA CLR
7. Press MODE RUN Indicator
8. Press GENL REG
9. Press DISPLAY NUMBER Indicator switches corresponding to octal value of bootstrap load channel.
10. Press PROG RUN
11. Press AUTO START SWITCH four times
12. If bootstrap load channel is a MIL-STD-188C or RS-232C or VACALES type channel, set ALTER MODE SET/CLR to CLR position.
13. Press DISPLAY SELECT CLR (Initiates Microdiagnostics)
14. PROG RUN lite extinguish
15. REGISTER/DATA = 070707. For any other value see technical manual.

## CP/MEMORY DIAGNOSTIC OPERATING PROCEDURES

1. Load CP/Memory Diagnostics
2. Press GEN REG and DISPLAY SELECT CLR. Display = 0
3. Press REG/DATA SET/CLR. Display (GR0) = 000000
4. Set PROGRAM STOP 1/OFF switch to OFF
5. Set PROGRAM STOP 2/OFF switch to 2
6. Set BOOTSTRAP 1/2 switch to down position
7. Press and observe GENL DSPL. Indicator III
8. Press REGISTER/DATA SET/CLR
9. Press REGISTER/DATA SET (P Reg.) switches 6 and 8 (000500)
10. Set AUTO START/START switches to START  
PROG RUN Indicator extinguished  
REGISTER/DATA = 000522
11. Set PROGRAM STOP 1/OFF switch to 1 and PROGRAM STOP 2/OFF switch to OFF
12. Set BOOTSTRAP 1/2 switch to up position
13. Set AUTO START/START to START  
PROG RUN Indicator extinguished  
REGISTER/DATA (P reg.) = 000532
14. Set AUTO START/START to START  
PROG RUN Indicator extinguished  
REGISTER/DATA (P reg.) = 000551
15. Press GENL REG
16. Press DISPLAY NUMBER switches for octal 04. Observe REGISTER/DATA (GR4) = 000000
17. Press DISPLAY NUMBER switches for octal 05. Observe REGISTER/DATA (GR5) = 000536
18. Press DISPLAY NUMBER switches for octal 07. Observe REGISTER/DATA (GR7) = 000546
19. Press GENL DSPL switch
20. Press DISPLAY SELECT CLR
21. AUTO START/START to START  
PROG RUN Indicator extinguished  
REGISTER/DATA (P reg.) = 000563
22. Set GR0, GR1, and GR2 to CP/Memory Configuration as follows:
 

GR0	Bit 0	Math Pac Installed
	Bit 1	Micro Growth Installed
	Bit 2	General Register set 2 Installed
	Bit 3	DMA Installed
	Bits 4-15	Not used
GR1	Bits 0-7	Memory Stacks Installed
GR2	Bits 0-7	Memory Stacks to be tested
23. Set both PROGRAM STOP switches to up position
24. Press GENL DSPL and DISPLAY SELECT CLR
25. Press AUTO START/START to START  
Observe PROG RUN Indicator  
REGISTER/DATA (P reg.):  
AN/UYK-20 = 000761  
AN/UYK-20A = 000765  
FAULT PROG Inc or Ill

## I/O DIAGNOSTIC PROGRAM OPERATING PROCEDURE

NOTE: If any common serial I/O channels are to be tested, ensure the zero/one fill option on the type 1/1A card (P/N 90536-7312528) is set to the one-fill mode (reference common serial mode selection instructions pages 39-42 of the Technical Summary).

- Load I/O Diagnostic
- Set switches to positions specified

INTERGMPTR TIME OUT	DOWN
GENL DSPL	SET
DISPLAY SELECT CLR	MOMENTARILY PRESSED
BOOTSTRAP 1/2	1
PROGRAM STOP 1/O/I	1
PROGRAM STOP 2/O/I	2
TEST/NORMAL ON I/O Mode Sel Card In DPS location 23C	TEST (LEFT POS) MOMENTARILY PRESSED
MA CLR	

- Set P = 500 Octal
- Press START
- Program stops at P = 510
- Set GR0 through GR17 to I/O channel availability and configuration and RTC Rates as determined by the I/O CHANNEL SELECTION TABLE (See page 61)
- Jumper channels
- Select P Reg
- Press START
- Program stops at P = 001063 (001073 for AN/UYK-20A)
- FAULT PROG should be lit.
- Set the TEST/NORMAL switch on I/O Mode Select card in DPS location 23C to NORMAL (right position).

## OPTIONS DIAGNOSTIC PROGRAM OPERATING PROCEDURE

A predetermined series of steps are required to initialize and execute the Options Diagnostic tests 1-6. These options are listed below in the order of execution.

TEST NUMBER	TEST NAME	MAX TIME (SEC)	
		UYK-20	UYK-20A
1	MATH PAC TEST	1	1
2	WORST CASE MEMORY TEST	45	90
3	SHIFTING BIT MEMORY TEST	30	160
4	GENERAL REGISTER GALPAT TEST	1	1
5	PAGE REGISTER GALPAT TEST	2	37
6	I/O CONTROL MEMORY GALPAT TEST	25	25
7	MAX BUFFER TEST	4	4
8	I/O CONCURRENT TEST	20	20
Total time approximately:		2 min.	6 min.

- Load the Options Diagnostic.
- Initial switch settings.

GENL DSPL	PRESS
DISPLAY SELECT CLR	PRESS
BOOTSTRAP 1/2	1
PROGRAM STOP 1/OFF	1
PROGRAM STOP 2/OFF	2
MA CLR	PRESS
TEST/NORMAL ON I/O MODE SEL CARD	TEST (LEFT POS)
IN DPS LOCATION 23C	

- Press and observe REGISTER/DATA Indicator-switches (P register) = 000500.
- Press AUTO START/START switch to START.
- Observe PROG RUN Indicator extinguished.
- Observe REGISTER/DATA Indicator-switches (P register) = 000512.
  - If correct, perform step 7.
  - If incorrect, suspect card is:

LOC	SWAP
A38	A24

The program has reached a parameter stop. If using a preinitialized tape and no parameter changes are to be made, omit steps 7 and 8.

- Set GR0 and GR1 to establish the appropriate equipment configuration to the program (see following Table).

## EQUIPMENT CONFIGURATION PARAMETERS

GENERAL REGISTER		CONFIGURATION
CP/MEMORY PARAMETERS		
GR0	BIT 0	MATH PAC INSTALLED
	BIT 1	MICRO GROWTH INSTALLED
	BIT 2	GENERAL REGISTER SET 2 INSTALLED
	BIT 3	DMA INSTALLED
	BIT 4-15	NOT USED
GR1	BIT 0-7	MEMORY STACKS INSTALLED

- Set GR3 and GR4 to select Options tests to be run and memory stack tests on which memory tests are to be run (see Table below).

## OPTIONS TEST SELECTION

GENERAL REGISTER		TEST SELECTED
OPTIONS PARAMETERS		
GR3	BIT 0	MATH PAC TEST
	BIT 1	MEMORY WORST CASE TEST
	BIT 2	MEMORY SHIFTING BIT TEST
	BIT 3	GENERAL REGISTER GALPAT TEST
	BIT 4	PAGE REGISTER GALPAT TEST
	BIT 5	I/O CONTROL MEMORY GALPAT TEST
	BIT 6	NOT USED
	BIT 7	MAX BUFFER TEST
GR4	BIT 8	I/O CONCURRENT TEST
	BIT 0-7	OPTIONS MEMORY STACKS TO TEST

- Press GENL DSPL Indicator-switch.
- Press DISPLAY SELECT CLR pushbutton.
- Press AUTO START/START switch to START.
- Observe PROG RUN Indicator extinguished.
- Observe REGISTER/DATA Indicator switches (P register) = 000520.

The program has reached another parameter stop. If using a preinitialized tape and no parameter changes are to be made, omit step 14.

- Set GR0 through GR17 corresponding to the I/O CHANNEL SELECTION TABLE. (See page 61).
- Press GENL DSPL Indicator-switch.
- Press DISPLAY SELECT CLR pushbutton.
- Press AUTO START/START switch to START position.
- Observe PROG RUN Indicator extinguished.
- Observe REGISTER/DATA Indicator switches (P register) = 000652.
- If Max Buffer Test was selected press AUTO START/START switch to START position. Observe PROG RUN Indicator is extinguished and REGISTER/DATA Indicator switches (P Register)=000724.
- If I/O Concurrent Test was selected, press AUTO START/START switch to START position. Observe PROG RUN Indicator is extinguished and REGISTER/DATA Indicator switches (P Register)=000737 with FAULT PROG Indicator lit.
- Press AUTO START/START switch to START position.
- Observe REGISTER/DATA Indicator switches (P Register)=001007.
- Set the TEST/NORMAL switch on I/O MODE SELECT CARD in DPS location 23C to NORMAL (Right Position).



# MICRO DIAGNOSTIC WITH END-AROUND JUMPERS OPERATING PROCEDURE

This procedure isolates and corrects malfunctions detected while attempting to bootstrap load diagnostic programs using micro diagnostic procedures.

## NOTE

Test not applicable if load channel is MIL-STD-188C, RS232C, VACALES or NTDS serial type interface.

1. Set POWER LOGIC ON/OFF switch to OFF.
2. Set TEST/NORMAL switch (on card in DPS location 23C) to TEST (left).
3. Disconnect load device from DPS connect output of load channel connector to its own input connector (see Page 24) using test I/O Jumper (P/N 90536-7150225-00, 90536-7150226-00, or 90536-7126394-00).

## NOTE

If loading was attempted on a 32-bit parallel channel, connect channel n, and remove dual channel jumper plugs from channel n+4.

4. Set POWER LOGIC ON/OFF switch to ON.
5. Press DISPLAY SELECT CLEAR pushbutton.
6. Press MODE MICRO STEP Indicator-switch.
7. Set DIAGNOSTIC DSPL switch to down position.
8. Set DIAGNOSTIC JUMP switch to up position.
9. Press MA CLR pushbutton.
10. Press MODE RUN Indicator-switch.
11. Press GENL DSPL Indicator-switch.
12. Set DISPLAY NUMBER to octal value of channel on which I/O Jumper cable is installed.
13. Press PROG RUN Indicator-switch.
14. Press AUTO START/START switch to START four times.
15. Press GENL REG Indicator-switch.
16. Press DISPLAY SELECT CLEAR pushbutton.
17. PROG RUN Indicator-switch extinguished. REGISTER/DATA = 070707.

I/O CHANNEL SELECTION TABLE FOR I/O DIAGNOSTIC PROGRAM EXECUTION

GENERAL REGISTER	I/O CONFIGURATION	CHANNEL NUMBER																	
		17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		SET BITS TO SELECT CHANNELS USED IN EACH CONFIGURATION																	
GR0	MIL-STD-1387 16-BIT PARALLEL CHANNELS (PIC, NTDS FAST, SLOW & ANEW)																		
GR1	MIL-STD-1387 32-BIT PARALLEL CHANNELS DUAL AND DUAL PIC																		
GR2	END-AROUND JUMPED CHANNELS FOR ALL CONFIGURED CHANNELS																		
GR3	MIL-STD-188C SERIAL CHANNELS (SYNCD & ASYNCD)																		
GR4	EIA-STD-RS-232C SERIAL CHANNELS (SYNCD & ASYNCD)																		
GR5	ASYNCHRONOUS CHANNELS (188C AND RS-232C)																		
GR6	MIL-STD-1387 NTDS SERIAL CHANNELS																		
GR7	MIL-STD-1387 ESA CHANNELS																		
GR10	MIL-STD-1387 NEW PIC CHANNELS (TYPE II)																		
GR11	VACUOL CHANNELS																		
GR12*	INTERNAL 1 KHz - SET BIT 2 RTC RATE 32 KHz - SET BIT 7 (SHADED BITS SHALL BE CLEARED)																		
GR13	MIL-STD-1387 OLD PIC CHANNELS (TYPE II)																		
GR16	EXTERNALLY CROSSED-CHANNELS JUMPED CHANNELS																		
GR17	CROSS-CHANNEL JUMPED SERIAL I/O CHANNELS																		

\* 1 KHz CLOCK = 7126200 PCB IN LOCATION B23  
32KHz CLOCK = 7127150 PCB IN LOCATION B23

NOTES

AN/UYK 20

I/O PINS:

5940-00-516-1702

NOTES